higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

NOVEMBER EXAMINATION

LOGIC SYSTEMS N6

29 NOVEMBER 2016

This marking guideline consists of 6 pages.

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QUESTION 1

1.1 True
Structured programming

1.2 True
Large-scale integration has been variously defined as bit density has increased over the last twenty years. This has made it difficult to be dogmatic about the correctness of different classifications. With millions of gates on one-chip Intel Pentium microprocessors fit into either of the two following classifications:

VLSI: Very Large Scale Integration
LSI: Large Scale Integration

1.3 True
A modem (acronym for modulator/demodulator) interfaces your computer with the telephone system so that you can use e-mail and connect to the internet.

True
1.4 A UART (universal asynchronous receiver/transmitter) is nowadays part of your modem card. It converts serial data (originally from the telephone line) to the parallel format used by your computer. It also converts parallel to serial in the other direction.

True
1.5 The operational amplifier is configured as a SUMMER.

True
1.6 The third state is: DISCONNECTION from the bus.

True
1.7 A port is a common interface.

False
1.8 There is no significant difference in stack use.

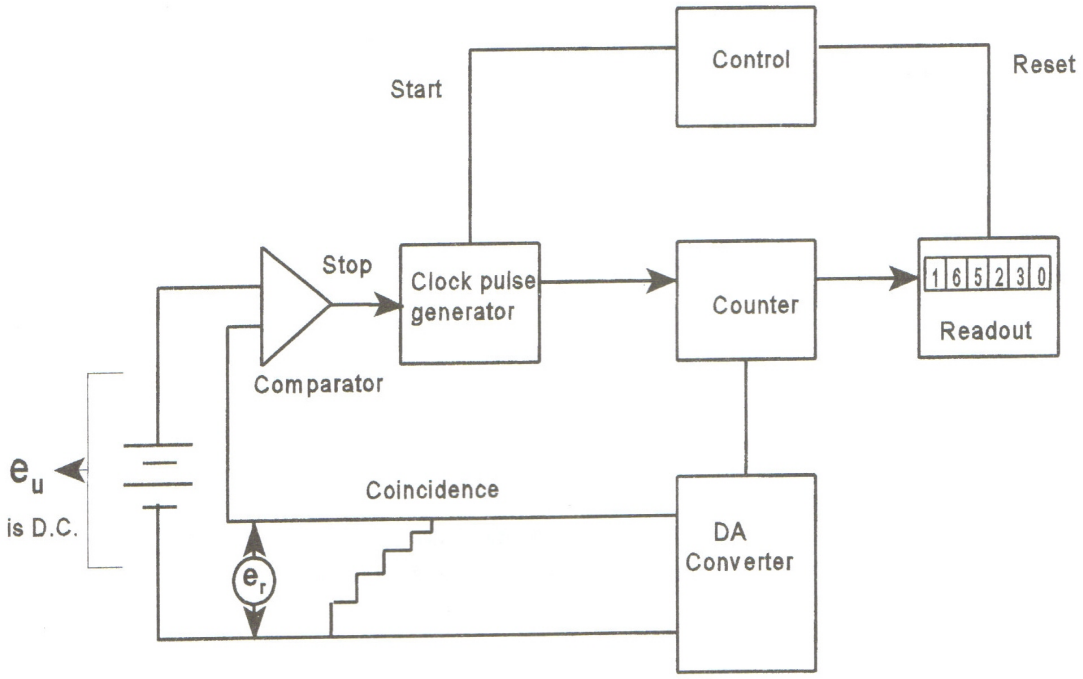
True
1.9 The ASCII code became a worldwide standard in the 1960s because of IBM's dominance of the computer market in those years.

False
1.10 A printer is not an interface. It is an output device.

(10 × 2) **[20]**

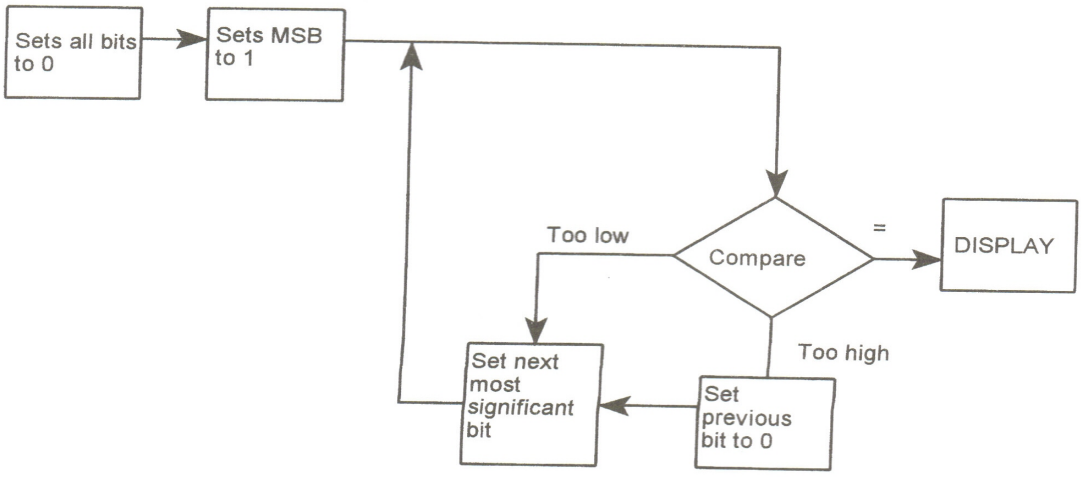
QUESTION 2

2.1



(10)

2.2



(9)

2.3 Assume a six-bit converter:

Clear register	000000	Binary input equivalent = 001000
Set MSB	100000	Too high clear bit and set next one
Reset and set next MSB	010000	Too high clear bit and set next one
Reset and set next MSB	001000	EQUALITY
Equality to input	001000	Equal to input so stop and **DISPLAY**

(6)
[25]

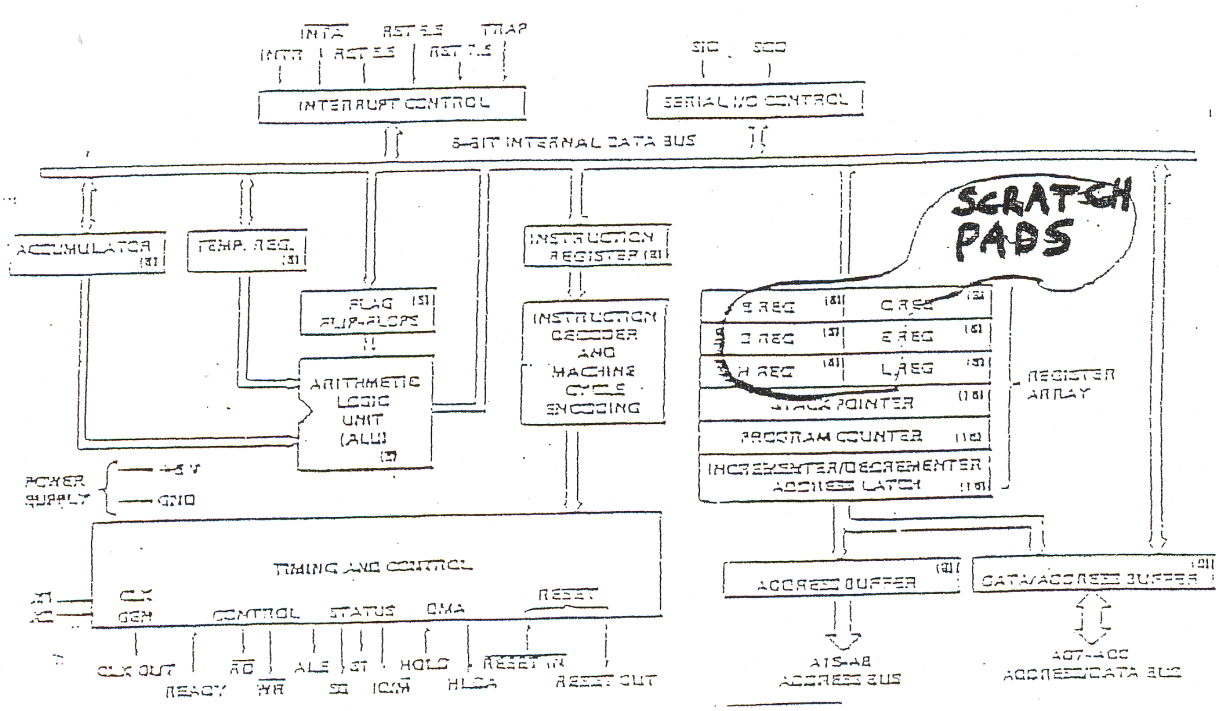
QUESTION 3

3.1 The major difference between Von Neumann Architecture and Harvard Architecture:

Von neumann architecture
Has only one memory – a RAM – so that the RAM is accessed twice during each machine cycle.
During the FETCH routine the ram is accessed to fetch the instructions routine into instructions register.
During the EXECUTE routine the RAM is accessed to get the operand out of the operand address.

Harvard architecture
Has two separate memories
RAM and ROM
One memory is usually EPROM or EEPROM which stores the program instructions permanently.
The RAM stores only the operands.
The FETCH and the EXECUTE routines will access two separate memories. (10)

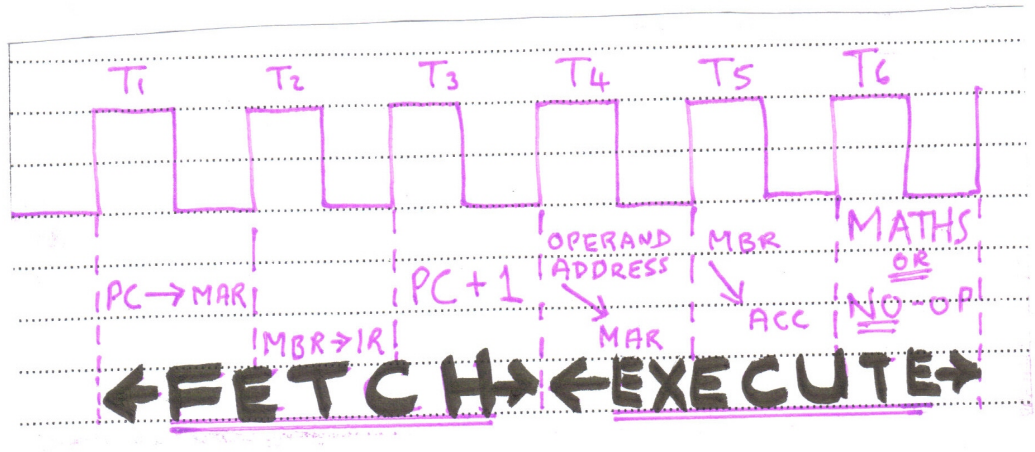
3.2 Intel 8085 CPU
Manufacturer: Intel Corporation



ALTERNATIVES ACCEPTED (10)
[20]

QUESTION 4

4.1 MACHINE CYCLE
The cycle (microinstruction cycle) in the control unit which carries out a PROGRAM INSTRUCTION (like 'LOAD').



(6)

4.2 4.2.1 Temporary data store during subroutines and interrupts (1)

4.2.2 Subroutines and interrupts (1)

4.2.3
- The stack stores active register data and the contents of the program counter (PC).
- On the 'RETURN' instruction, this data is returned to the original registers so that the main program can be resumed. (4)

4.3

INSTRUCTION LOCATION	INSTRUCTION WORD		DESCRIPTION
	OP CODE	ADDRESS	
CCCA	LOAD	F1B4	Load u✓
CCCB	ADDA	F1B3	Add t✓
CCCC	BARP	CCD1✓	Branch if Acc > C✓
CCCD	MULT	F1B4	Multiply by u✓
CCCE	BRAP	CCD1✓	Branch if Acc > O✓
CCCF	STOR	F1B9	Store in z✓
CCD0	OUTP		Output✓
CCD1	HALT		Halt✓

(10)
[20]

QUESTION 5

5.1 The gain of a non-inverting operational amplifier must always be greater than one.

In this circuit the gain is less than one and therefore the operational amplifier is faulty and must be replaced.

INPUT	×	GAIN	=	OUTPUT
12 volts	×	0,5	=	6 volts

(Gain = 0,5: which is less than one. So: Change the Op Amp!) (6)

5.2

ADVANTAGES	DISADVANTAGES
• Only two resistor values needed✓✓ • The range of the converter is easily extended✓ • Nonstandard resistors can be used✓✓	• Cannot convert BCD✓

(6)

5.3 Increase the number of bits in the register. (3)

[15]

TOTAL: 100

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