higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N6

3 APRIL 2020

This marking guideline consists of 5 pages.

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QUESTION 1

1.1 False
- Do not require power to retain data
- Nonvolatile
- Stores data permanently (Any 2 × 1)

1.2 True
The debouncing circuit prevents multiple microclosures of contacts so that pressing a particular key registers only one single contact.

1.3 False
Low-level programming language.

1.4 True
A magnetic tape is read serially so that data is accessed in sequential order.

1.5 True
The operational amplifier is configured as a series adder.

1.6 True
The tristate device can disconnect from the bus as the third state.

1.7 True
A USB port is a common interface (both input and output) to outside devices.

1.8 False
Stack usage is the same. There is no significant difference in stack use.

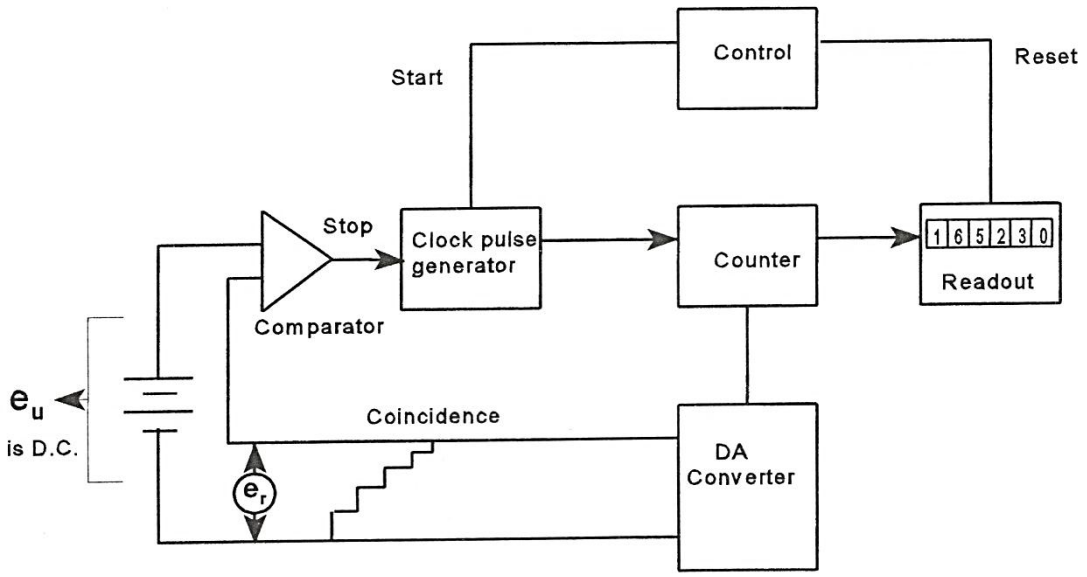
1.9 False
The ASCII code became a worldwide standard in the 1960's and remains so because of IBM's dominance of the computer market.

1.10 False
A graph plotter is an output device.

(10 × 2) **[20]**

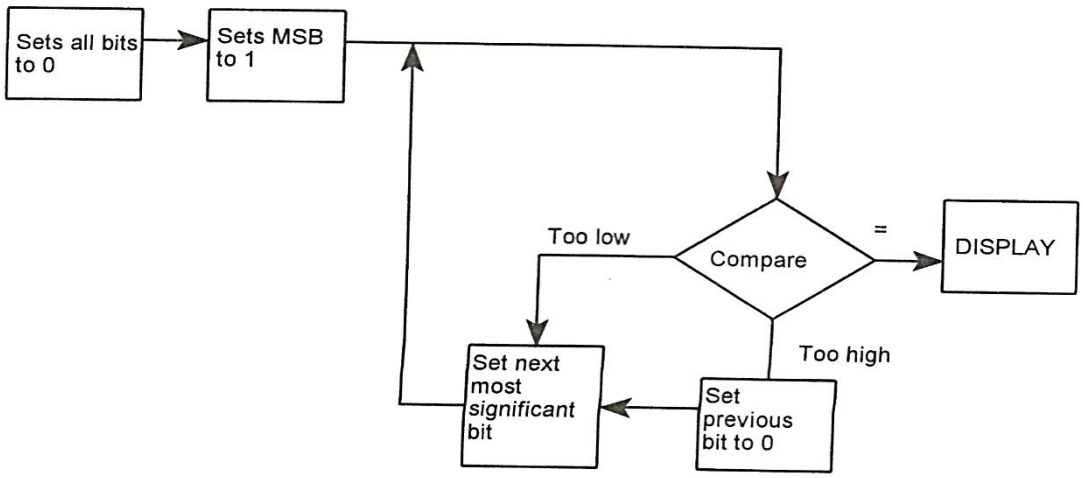
QUESTION 2

2.1



(10)

2.2



(9)

2.3 SIX-BIT CONVERTER

Clear register:	000000✓	**Binary input equivalent = 001011✓**
Set MSB	100000	Too high clear bit and set next one✓
Reset and set next MSB	010000	Too high clear bit and set next one
Reset and set next MSB	001000	Too low keep bit and set next MSB✓
Set next MSB	001100	Too high clear bit and set next MSB
Reset and set next MSB	001010	Too low keep bit and set next MSB
Set next MSB	001011	Equal to input so stop and display✓

Equal to input so stop and display✓ (6)

[25]

QUESTION 3

3.1 Von Neumann architecture:

- Has only one memory – a RAM – so that the RAM is accessed TWICE during each machine cycle.
- During the FETCH routine the RAM is accessed to fetch the instructions routine into the INSTRUCTIONS REGISTER.
- During the EXECUTE routine the RAM is accessed to get the operand out of the operand address.

Harvard architecture:

- Has two separate memories,
- RAM and ROM.
- One memory is usually EPROM or EEPROM which stores the program instructions permanently.
- The RAM stores only the operands.
- The FETCH and the EXECUTE routines will access two separate memories. (10)

3.2

LETTER	BINARY VALUE	BCD VALUE
A	100 0001✓	41✓
B	100 0010✓	42✓
C	100 0011✓	43✓
D	100 0100✓	44✓
E	100 0101✓	45✓

(5 × 2) (10)
[20]

QUESTION 4

4.1 A D/A converter converts digital inputs to an equivalent analogue output value.

An A/D converter converts an analogue input value to an equivalent digital (binary) value. (6)

4.2 The accumulator stores ongoing results from the output of the ALU after each calculation or computation. Data (results) in the accumulator can then be stored in memory. (4)

4.3 **PROGRAM**

INSTRUCTION LOCATION	INSTRUCTION WORD		DESCRIPTION
	OPCODE	ADDRESS	
FCCA	LOAD	F1B4	Load u✓
FCCB	SUBT	F1B3	Subtract t✓
FCCC	BRAN	FCD1 ✓	Branch if Acc. < 0✓
FCCD	MULT	F1B4	Multiply by u✓
FCCE	BRAN	FCD1 ✓	Branch if Acc. < O✓
FCCF	STOR	F1B9	Store in z✓
FCD0	OUTP		Output✓
FCD1	HALT		Halt✓

NOTE that other programming sequences are also accepted. (10)
[20]

QUESTION 5

5.1 The gain of this inverting operational amplifier must be greater than one since the question states that it must amplify the signal.

In this circuit the gain is less than one and the output is not inverted from the input. Therefore, the operational amplifier is faulty and must be replaced.

INPUT	X	GAIN	=	(inverted) OUTPUT
✓	✓	✓	✓	✓✓

(6)

5.2

ADVANTAGES	DISADVANTAGES
Only two resistor values needed, R and 2R.✓✓	Cannot convert BCD.✓
The range of the converter is easily extended.✓	
Nonstandard resistors can be used.✓✓	

(6)

5.3 Increase the number of bits in the register. (3)
[15]

TOTAL: 100

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