higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

# MARKING GUIDELINE

## NATIONAL CERTIFICATE

## APRIL EXAMINATION

## LOGIC SYSTEMS N6

## 11 APRIL 2016

**This marking guideline consists of 10 pages.**

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## QUESTION 1

1.1 The International Electrotechnical Commission (IEC) is the world's leading organisation that prepares and publishes international standards for all electrical, electronic and related technologies. (5)

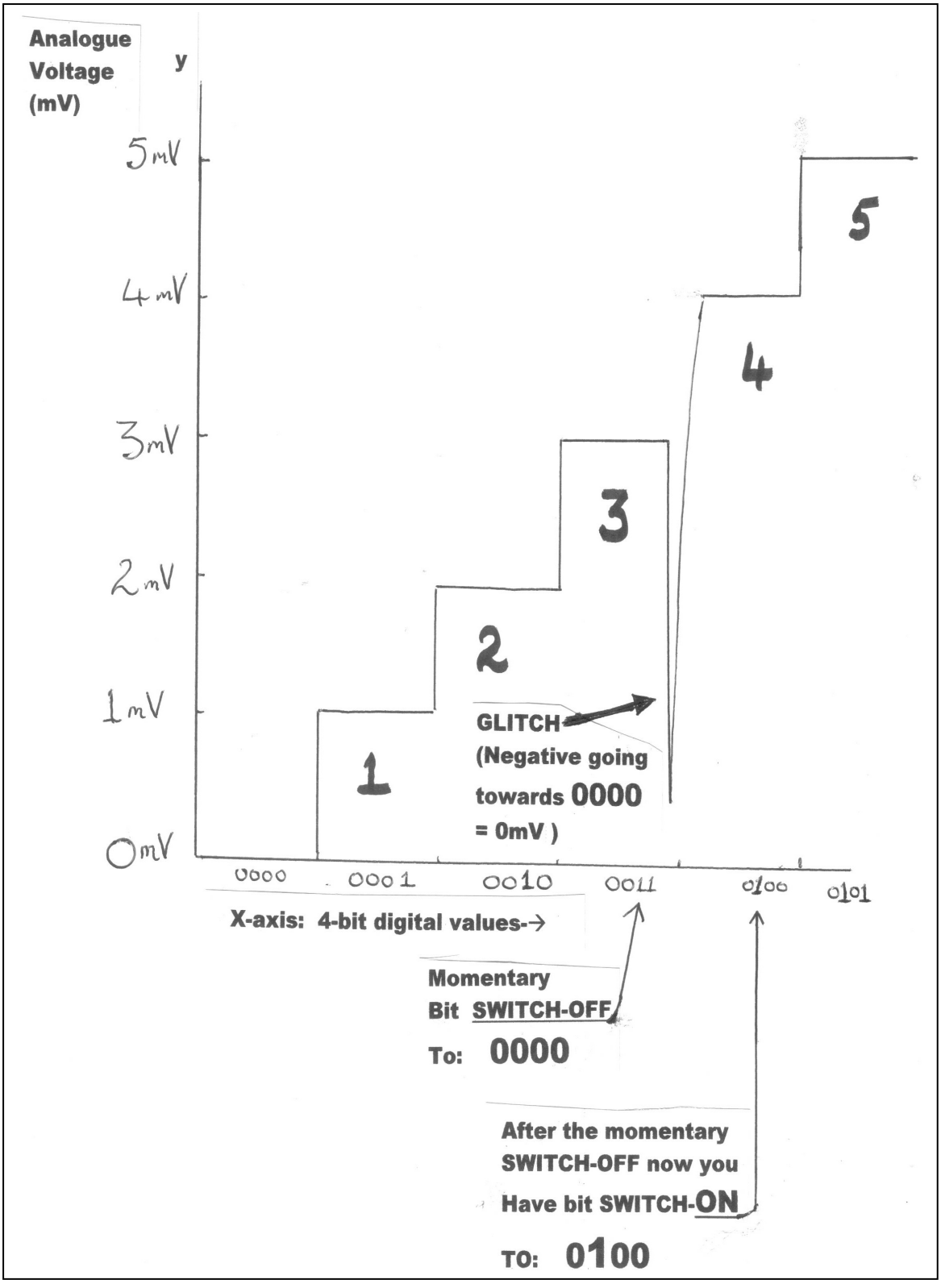
1.2 The International Electrotechnical Commission (IEC) is one of three global sister organisations (IEC, ISO, ITU) that develop international standards for the world. Each member country has one vote and a say in each IEC international standard. (5)

1.3 Millions of devices that contain electronics, and use or produce electricity, rely on IEC international standards and conformity assessment systems. By complying with IEC international standards these millions of devices perform, fit and work safely together. South Africans designing or using logic systems (hardware or software) must conform to IEC standards to run their own industries and to export to the world. The IEC open international standard IEC 61131 is of particular importance in this regard. (5)

1.4 Glitches are high-frequency voltage spikes (sometimes very large) which occur in the output of a digital-to-analogue converter for some changes in the input.

The glitch shown below which deforms the up-count output of a digital-to-analogue converter (DAC) takes place because the time that the DAC components take to switch off is quicker than their switch-on time. As is illustrated in the graph below this results in a deformation of the step waveform between count 3 and count 4. The voltage spikes suddenly towards 0 mV before recovering at switch-on.

Components generally take longer to switch on than to switch off. Semiconductor components need to energise charge carriers when they switch on and this takes time.


Analogue Voltage (mV)
y
5mV
4mV
3mV
2mV
1mV
0mV
1
2
3
4
5
GLITCH
(Negative going towards 0000 = 0mV )
0000
0001
0010
0011
0100
0101
X-axis: 4-bit digital values-→
Momentary Bit SWITCH-OFF To: 0000
After the momentary SWITCH-OFF now you Have bit SWITCH-ON TO: 0100

√
√
√
√
√

(5)
**[20]**

**QUESTION 2**

2.1 2.1.1 The simplest mathematical form of the equation which this program segment solves:

Y = r + r + r + r + r -- s –– s – s + t + t + t + t

Y = 5r - 3s + 4t (4)

2.1.2 The language used to write this programming segment:

ASSEMBLER (which uses mnemonics like: ADDA, MULT and so on). (4)

2.1.3 Showing ALL STEPS to calculate the decimal output of the program segment:

Y = 5(F1B1) -- 3(F1B2) + 4(F1B3)

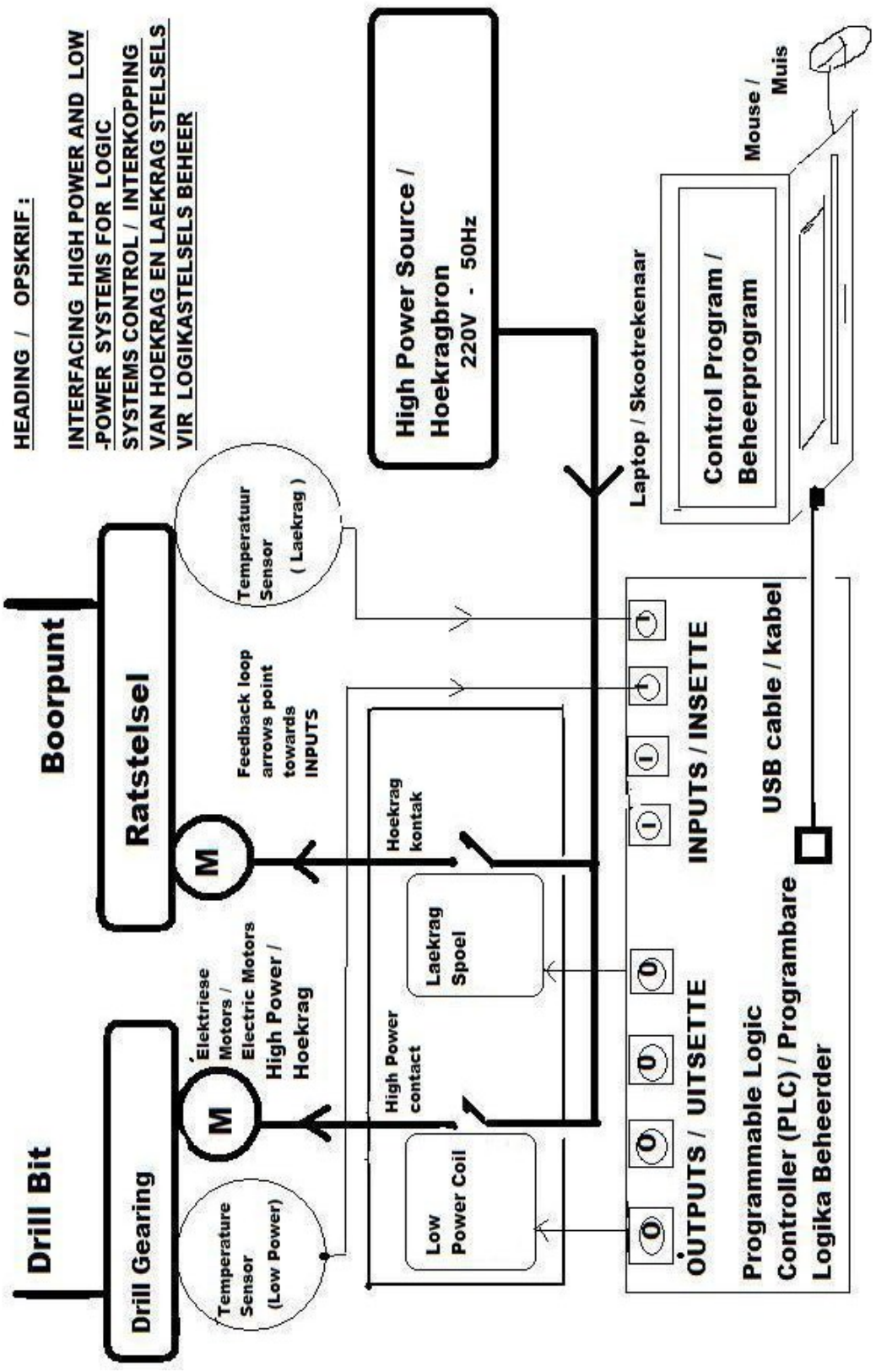
Y = 5r -- 3s + 4t

Y = 5(1100) -- 3(1000) + 4(900)

Y = 5500 -- 3000 + 3600

Y = 6100 (DECIMAL) (2)

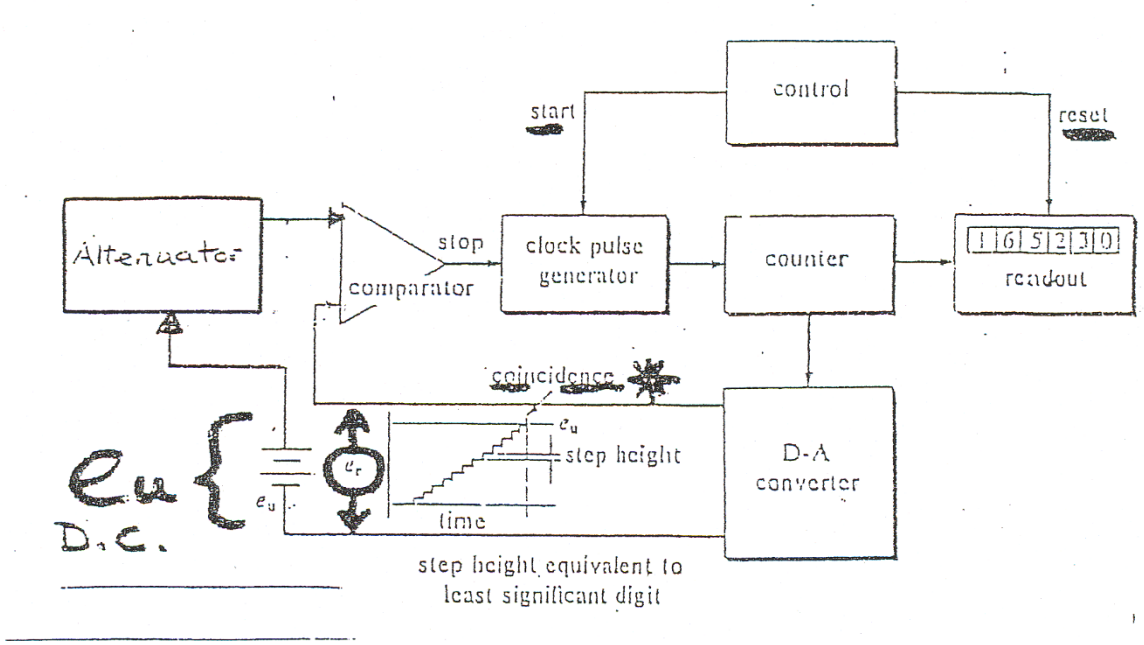
2.2


HEADING / OPSKRIF:
INTERFACING HIGH POWER AND LOW -POWER SYSTEMS FOR LOGIC SYSTEMS CONTROL / INTERKOPPING VAN HOEKRAG EN LAEKRAG STELSELS VIR LOGIKASTELSELS BEHEER
Drill Bit
Drill Gearing
Boorpunt
Ratstelsel
Elektriese Motors / Electric Motors
High Power / Hoekrag
M
M
Temperature Sensor (Low Power)
Temperatuur Sensor ( Laekrag )
Feedback loop arrows point towards INPUTS
High Power contact
Low Power Coil
Hoekrag kontak
Laekrag Spoel
OUTPUTS / UITSETTE
INPUTS / INSETTE
Programmable Logic Controller (PLC) / Programbare Logika Beheerder
USB cable / kabel
High Power Source / Hoekragbron 220V - 50Hz
Laptop / Skootrekenaar
Control Program / Beheerprogram
Mouse / Muis

(10)
**[20]**

## QUESTION 3

3.1 STAIRCASE RAMP ANALOGUE-TO-DIGITAL CONVERTOR: BLOCK DIAGRAM




(7)

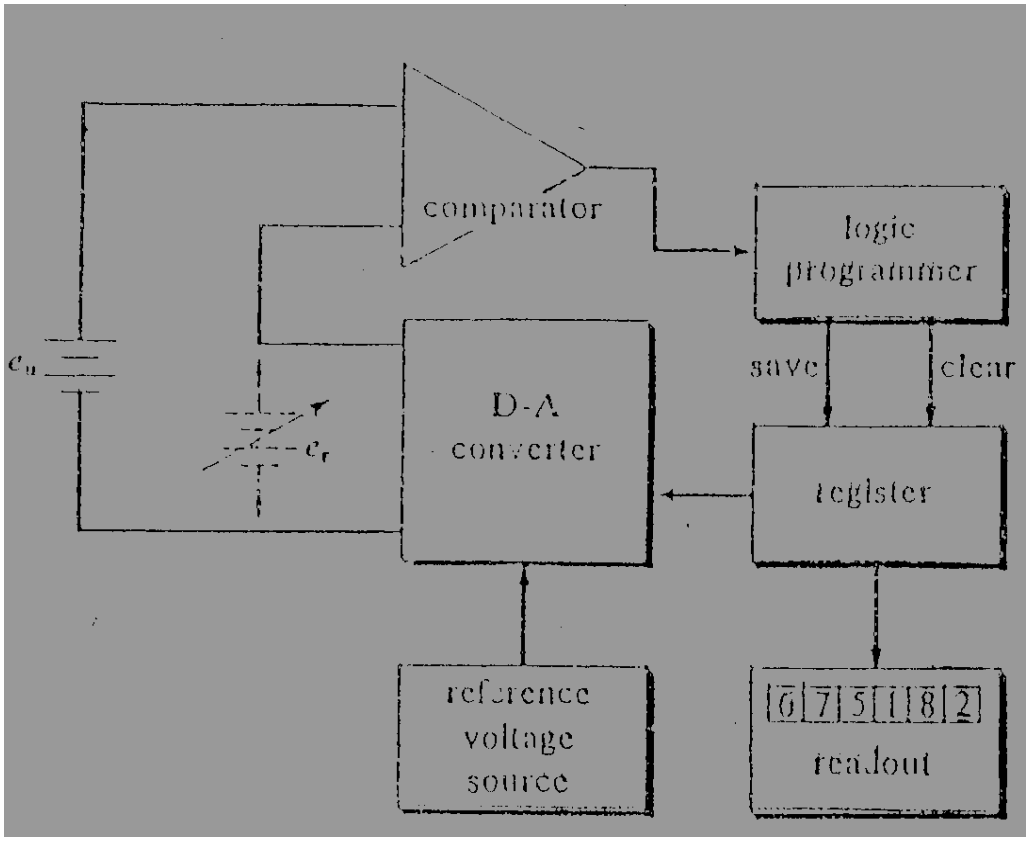
3.2 DISADVANTAGE OF THE STAIRCASE RAMP ADC IN COMPARISON WITH THE SUCCESSIVE-APPROXIMATION ADC:

The disadvantage of the staircase ramp ADC in comparison with the successive- approximation ADC is that it is slower.

The reason for this is as follows:
The staircase ramp uses a counter (which increments the LSB) to count up to the input voltage. If the input voltage is high then the count (and the upward moving staircase towards that value) can take a long time.

The successive-approximation ADC uses a register instead of a counter. This allows the MSB (most significant bit) to be set and this saves the long time that a count can take. (7)

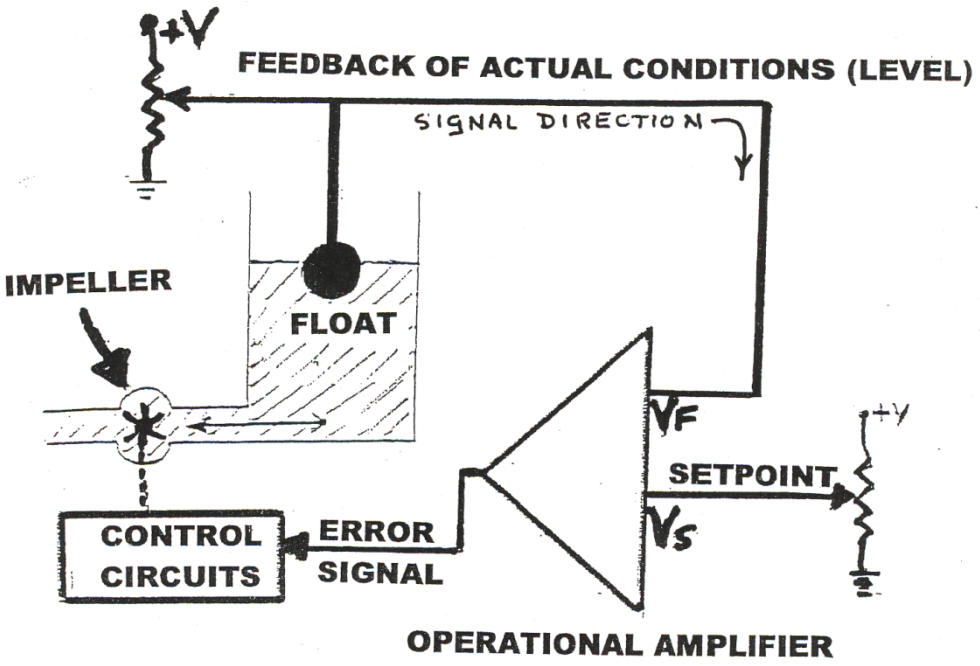
3.3 BLOCK DIAGRAM OF THE SUCCESSIVE-APPROXIMATION ADC




(6)
**[20]**

**QUESTION 4**

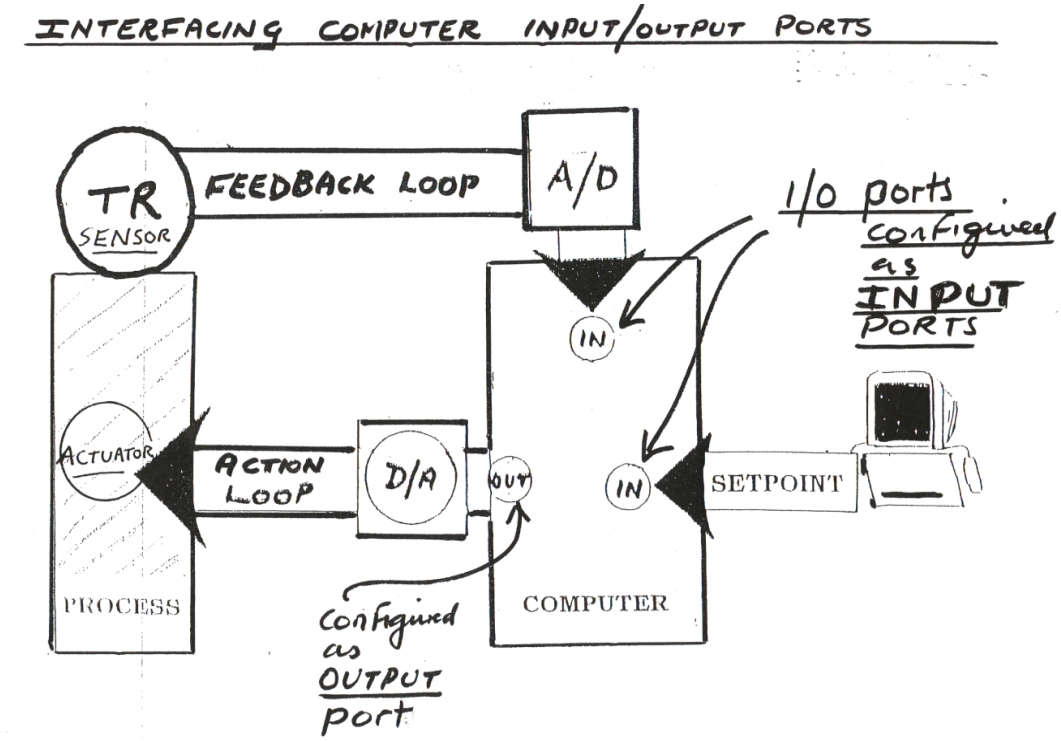
4.1 CONTROL OF TANK-LEVEL USING AN OP-AMP COMPARATOR




The above circuitry and process blocks show an analogue control system using an operational amplifier.

- When VF = S then the ERROR SIGNAL = 0 and the pump impeller does not move.
- When VF ≠ VS than the ERROR SIGNAL causes the bi-directional pump impeller to turn until set-point level is realised. (9)

4.2




(9)

4.3 PLC TOGGLING FROM STATEMENT LIST TO DIAGRAM MODE:

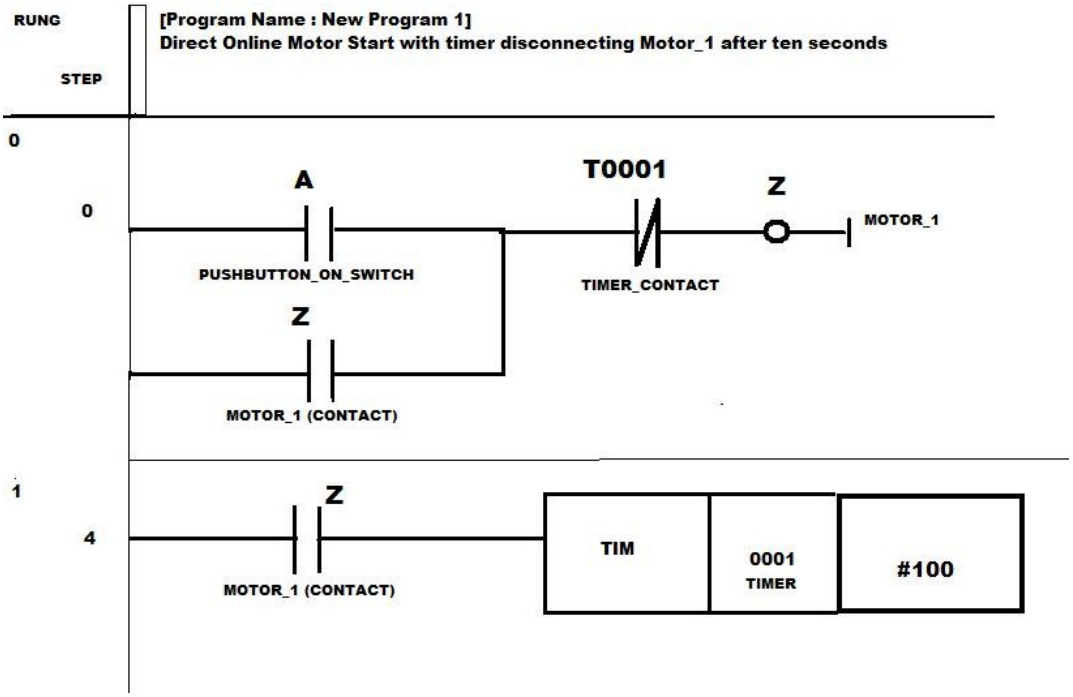
When the statement list mnemonic 'OR' is displayed in ladder diagram, the ladder diagram shows the inputs in parallel. (2)
**[20]**

## QUESTION 5

5.1 The programming languages defined by the International Electrotechnical Commission under open international standard IEC 61131-3. (Format: text or graphical)

(1) Ladder diagram (graphical)
(2) Function block diagram (graphical)
(3) Structured text (text)
(4) Instruction list (text)
(5) Sequential function chart (graphical) (10)

5.2




(10)
**[20]**

**TOTAL: 100**

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