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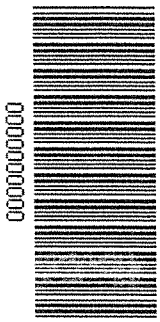

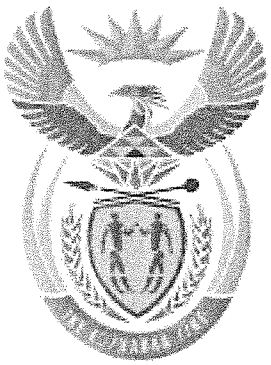

higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T900(E)(A7)T

APRIL EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N6

(8080306)

7 April 2015 (Y-Paper)
13:00–16:00

Calculators may be used.

This question paper consists of 7 pages.

ENGINEERING

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N6
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Substantiate your work with authoritative and easily checkable website links where necessary
5. Write neatly and legibly.

NOTICE TO CANDIDATES

The lives and safety of people depend on logic systems. Logic systems prevent lift doors from crushing persons to death. Logic signalling systems prevent trains from colliding. Logic systems keep people safe in aircraft and in hospital intensive-care units. Your work, programming and designs, must be properly planned and presented at this Diploma-level examination. Standards must be maintained for the safety of the public.

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QUESTION 1

1.1 The program segment below is given in Instruction List (also commonly called 'Statement List'). The program allows MOTOR_1 to run for ten seconds (#100) before it is disconnected by TIMER_1. The values given in the VALUE column are (with the exception of the hexadecimal timer value) Boolean values (either 0 or 1). The values given in the table are the un-energised values before the circuit is switched on. Draw the Ladder Diagram format of this program segment. Place addresses above each component. Place comments under each component.

RUNG	STEP	INSTRUCTION	OPERAND	VALUE	COMMENT
0	0	LD	**A**	0	PUSHBUTTON ON_SWITCH
	1	OR	**Z**	0	MOTOR_1 (CONTACT)
	2	ANDNOT	**T0001**	0	TIMER CONTACT
	3	OUT	**Z**	0	MOTOR_1
1	4	LD	**Z**	0	MOTOR_1 (CONTACT)
	5	TIM	**0001**	0100 Hex	TIMER_1
			#100		

(10)

1.2 List the programming languages defined by the International Electrotechnical Commission under Open International Standard IEC 61131-3. Clearly show the programming format of each language (i.e. text or graphical). (10)

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QUESTION 2

2.1 An electrician, millwright or Logic Systems Engineer must be able to use input and output ports to run external operations. It is also necessary to interface low-power logic systems control signals with high power current and voltage in order to perform external operations. Draw a large neat fully-labelled block diagram to show how you would use a USB to connect your laptop to a Programmable Logic Controller (PLC) with four input and four outputs. This connection allows you to download your program from your laptop to the PLC. Show the necessary connections from the PLC to a relay bank with two relays. Each relay switches high power to each of two motors which run two drills. Carefully draw the feedback loops which trip the motors whenever the temperature of the drills' gearing exceeds the set point you have set in your PLC program. Show ALL signal directions. Clearly distinguish low power lines and components from high power lines and components. Label feedback loops. In this examination question you need not show Analogue-to-Digital (ADC) or Digital-to-Analogue (DAC) conversions as process blocks. It will be accepted that those conversions will be done as software conversions programmed by you to operate within the PLC. (10)

2.2 **PROGRAMMING INSTRUCTION PROCEDURE**

Given below is a program segment together with accompanying INSTRUCTION SET and Information about Pre-Loaded Addresses. Analyse this given information to answer the questions which follow.

INSTRUCTION LOCATION/ INSTRUKSIE-ADRES	INSTRUCTION WORD/ INSTRUKSIEWOORD		DESCRIPTION/ BESKRYWING
	OP-CODE OP-KODE	ADDRESS/ ADRES	
AAAA	LOAD	F1B1	Load r
AAAB	ADDA	F1B1	Add r
AAAC	ADDA	F1B1	Add r
AAAD	ADDA	F1B1	Add r
AAAE	ADDA	F1B1	Add r
AAAF	SUBT	F1B2	Subtract s
AAB0	SUBT	F1B2	Subtract s
AAB1	SUBT	F1B2	Subtract s
AAB2	ADDA	F1B3	Add t
AAB3	ADDA	F1B3	Add t
AAB4	ADDA	F1B3	Add t
AAB5	ADDA	F1B3	Add t
AAB6	STOR	F1B8	Store in y (new value)
AAB7	OUTP		Output
AAB8	HALT		Halt

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The following INSTRUCTION SET is available:

OP-CODE	DESCRIPTION
LOAD	Load accumulator
ADDA	Add to accumulator
SUBT	Subtract from accumulator
MULT	Multiply
BRAN	Branch if the accumulator is negative
BRAP	Brings if the accumulator is positive
STOR	Store
OUTP	Output the contents of the accumulator
HALT	Halt (non-memory referenced instruction)

Information about Pre-loaded Addresses:

The operands r, s, t, u v, w, x, y and z are stored in consecutive hexadecimal addresses:

Operand r is stored in address F1B1
Operand s is stored in address F1B2
Operand t is stored in address F1B3
Operand u is stored in address F1B4 - and so on.

The value of 'r' is pre-loaded with the decimal integer value 1 100
The value of 's' is pre-loaded with the decimal integer value 1 000
The value of 't' is pre-loaded with the decimal integer value 900
The value of 'u' is pre-loaded with the decimal integer value 800

The integer values pre-loaded into the alphabetical variables which follow 'u' continue to decrement by 100 so that 'z' is pre-loaded with decimal 300

2.2.1 Write in your ANSWER BOOK (under an appropriate heading) the simplest mathematical form of the equation which this program segment solves. (4)

2.2.2 Write in your ANSWER BOOK (under an appropriate heading) what sort of programming language has been used to write this program segment (i.e. Machine Code, Assembler, BASIC, COBOL, C++, Ruby-on-Rails, or other). (4)

2.2.3 Write in your ANSWER BOOK (under an appropriate heading) the value (numerical or otherwise) printed out on completion of this program segment.

Show ALL steps in your calculation. (2)
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QUESTION 3

3.1 Draw a complete fully-labelled block diagram of a STAIRCASE RAMP analogue-to-digital converter. Also draw the staircase voltage waveform. Clearly show where the staircase voltage waveform originates and to which component it is connected. (7)

3.2 Discuss the disadvantage of the staircase ramp analogue-to-digital converter in comparison with the successive-approximation analogue-to-digital converter. Clearly explain what component is changed (and to what it is changed) in the successive- approximation ADC to make it a more effective ADC than the staircase ramp. (7)

3.3 Draw a complete fully labelled block diagram of the successive-approximation analogue-to-digital converter. (6)
[20]

QUESTION 4

4.1 A programmer is able to program a PLC (Programmable Logic Controller) using either DIAGRAM mode or MNEMONICS (STATEMENT LIST). Clicking on icons gives the programmer the choice of display. Describe the form of circuit diagram which is displayed to represent an 'OR' statement. (2)

4.2 Draw a large neat fully labelled diagram of an operational amplifier configured as a comparator. The operational amplifier is used to control the level of liquid in a tank. Show the connections to sensor(s) and actuator(s) necessary to control the level. Show signal directions. Show any analogue-to-digital or digital-to-analogue converters that may be needed. Fully integrate the control circuitry with the objects which are being controlled. (9)

4.3 Draw a large, neat, fully labelled block diagram to show the interfacing of input/output ports of a computer. The computer is used to control the level of liquid in a tank. The labels of the block diagram must appear on the block diagram itself. Clearly show the configuration of each input/output port. All interfacing and process functions needed to monitor and control the level must be shown. Show signal directions. Show the interfacing of sensor(s) and actuator(s). Label the feedback and action loops. (9)
[20]

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QUESTION 5

5.1 To demonstrate why a glitch can appear in a Digital to Analogue Convertor you are asked to do the following: Draw the staircase output waveform of a 4-bit digital to analogue converter. The staircase output detailed on the vertical axis must indicate increasing analogue values from 0 mV to 5 mV. Clearly show the corresponding 4-bit digital values on the horizontal axis. Assume that only ONE glitch occurs between steps three and four because bit switch-on takes longer than bit switch-off. Draw this glitch superimposed on the staircase waveform. Clearly show the shape and direction of the glitch as it appears on an oscilloscope screen. Enter the momentary value which causes the glitch and show between which values this momentary value appears. (5)

5.2 What is the International Electrotechnical Commission (I.E.C.)? Describe its functions and its worldwide importance. (5)

5.3 Describe why the International Electrotechnical Commission (I.E.C.) is a truly international organization. (5)

5.4 What relevance does the International Electrotechnical Commission (I.E.C.) have for Logic Systems in the South African context? (5)

[20]

TOTAL: 100

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