higher education & training

Department:
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NATIONAL CERTIFICATE

LOGIC SYSTEMS N5

(8080295)

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09:00–12:00

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N5
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. ALL circuits must be fully labelled.
5. Binary registers should be drawn with the most significant bit (MSB) flip-flop on the left and the least significant bit (LSB) flip-flop on the right.
6. Waveforms should be drawn with the clock input on top followed by the LSB flip-flop output below the clock input and with the MSB flip-flop output as the last output waveform at the bottom.
7. Write neatly and legibly.

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QUESTION 1

A conveyer belt control circuit requires a binary counter which counts as follows:

0_{10}, 1_{10}, 3_{10}, 7_{10}, 6_{10}, and 4_{10}

Design a *synchronous* binary counter that produces the above count cycle.

The counter must be self-starting and must exit from any unused state to the starting state within ONE clock pulse.

Design and draw the circuit making use of JK master/slave flip-flops. **[15]**

QUESTION 2

A guillotine safety circuit needs to generate a count cycle which is as follows:

2_{10}, 3_{10}, 4_{10}, and $5_{10.}$

Draw the truth table, the circuit and the input and output waveforms for an *asynchronous* binary counter which uses gated reset/set to produce the above count cycle.

Use JK master/slave flip-flops in the circuit.

The truth table and waveforms must clearly show the reset action. **[15]**

QUESTION 3

Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (3.1–3.13) in the ANSWER BOOK.

3.1 Multiplexing could be regarded as a form of 'time share'.

3.2 Multiplexing eliminates all but one of the data transmission lines.

3.3 The purpose of multiplexing is to reduce the number of transmission lines.

3.4 The purpose of multiplexing is to increase the number of transmission lines.

3.5 A 4 to 1 multiplexor has 1 data input and 4 transmission lines.

3.6 A 4 to 1 multiplexor has 4 data inputs and 1 transmission line.

3.7 A 1 to 4 demultiplexor has 4 data inputs and 1 output data bit.

3.8 A 1 to 4 demultiplexor has 1 data input and 4 output data bits.

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3.9 Only the multiplexor requires a sequencer.

3.10 Only the demultiplexor requires a sequencer.

3.11 Both the multiplexor and the demultiplexor require a sequencer.

3.12 The multiplexor and demultiplexor need to be synchronised.

3.13 The disadvantage of multiplexing is a slower transmission speed.

(13 × 1) **[13]**

QUESTION 4

Shift registers are designed to store data temporarily and to shift the stored data either to the left or to the right.

4.1 Draw a neat, fully labelled circuit diagram of a four-bit parallel-input serial-output (PISO) shift left register. Show ALL the relevant connections. (9)

4.2 Indicate whether the shift register in QUESTION 4.1 will make use of ASYNCHRONOUS clocking or SYNCHRONOUS clocking. (1)

4.3 Identify the number of inputs you will have at the input of the shift register in QUESTION 4.1. (1)

4.4 Identify the number of outputs you will have at the output of the shift register in QUESTION 4.1. (1)

[12]

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QUESTION 5

Choose a description or an answer from COLUMN B that matches an item or a problem in COLUMN A. Write only the letter (A–O) next to the question number (5.1–5.15) in the ANSWER BOOK.

COLUMN A		COLUMN B	
5.1	5_{10} plus 7_{10} in XS3BCD is …	A	… adds or subtracts 2 multibit numbers using 1's complement.
5.2	5_{10} plus 7_{10} in 8421BCD is …	B	… a shift left and subtract process.
5.3	1100_2 plus 1001_2 plus 0110_2 is …	C	… adds two bits plus a carry-in.
5.4	1101_2 times 101_2 is …	D	… is slower than the parallel ALU.
5.5	11101_2 minus 10100_2 is …	E	… a shift right and add technique.
5.6	The 2's complement of negative 011010 is …	F	… stands for arithmetic logic unit.
5.7	The 1's complement of negative 011010 is …	G	… adds two multibit numbers.
5.8	ALU …	H	… adds or subtracts 2 multibit numbers using 2's complement.
5.9	The full adder …	I	… $01001_{2.}$
5.10	The parallel adder…	J	…$100110_{2.}$
5.11	The parallel 1's complement ALU …	K	…0100 0101.
5.12	The parallel 2's complement ALU …	L	…$100101_{2.}$
5.13	The multiplication process is …	M	…0001 0010.
5.14	The division process is …	N	…$1000001_{2.}$
5.15	The series adder ALU …	O	…$11011_{2.}$

(15 × 1) (15)
[15]

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QUESTION 6

Answer QUESTIONS 6.1–6.7 by choosing memory types from the list (A–H) below. Choose the answer and write only the letter or letters (A–H) next to the question number (6.1–6.7) in the ANSWER BOOK.

A PROM
B SRAM
C DRAM
D Hard disk
E Magnetic drum
F Magnetic core
G Magnetic tape
H None

6.1 Choose any TWO of the above memories that are semiconductor types. (2)

6.2 Which of the above memories are volatile? (2)

6.3 Which of the above memories are non-volatile? (5)

6.4 Which of the above memories are dynamic? (1)

6.5 Which of the above memories are static? (2)

6.6 Which of the above memories are no longer used? (2)

6.7 Which of the above memories require refreshing circuits? (1)
[15]

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QUESTION 7

Printers are output devices that convert soft copy into hard copy.

Answer QUESTIONS 7.1–7.6 by choosing printer types from the list (A–I) below. Choose the answer and write only the letter or letters (A–I) next to the question number (7.1–7.6) in the ANSWER BOOK.

A. Static printer
B. Inkjet printer
C. Graph plotter
D. Chain printer
E. Thermal printer
F. Dot matrix printer
G. Laser printer
H. Drum printer
I. None

7.1	Identify TWO printers that print pre-formed characters.	(2)
7.2	Identify THREE impact printers.	(3)
7.3	Identify FIVE non-impact printers.	(5)
7.4	Identify THREE printers that can print in colour.	(3)
7.5	Identify the printer that can print on the largest paper size.	(1)
7.6	Identify the printer with the highest printing speed.	(1)
		[15]

TOTAL: 100

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