higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T800**(E)**(N25)T

NOVEMBER EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

25 November 2016 (X-Paper)
09:00–12:00

Calculators may NOT be used.

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Keep questions and subsections of questions together.
5. ALL the sketches and diagrams must be large, clear and neat.
6. Show ALL the steps and calculations.
7. Write neatly and legibly.

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QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

1.1 Convert each of the following numbers to their BINARY equivalents and then complete the calculations in the binary number system:

1.1.1 $10_8 \times F_{16}$ (4)

1.1.2 $51_{16} \div 9_{10}$ (5)

1.2 Subtract 71_8 from $1\ 0\ 1\ 0\ 1\ 1_2$ using the 2's complement method. (4)

1.3 Study FIGURE 1 and answer the questions.

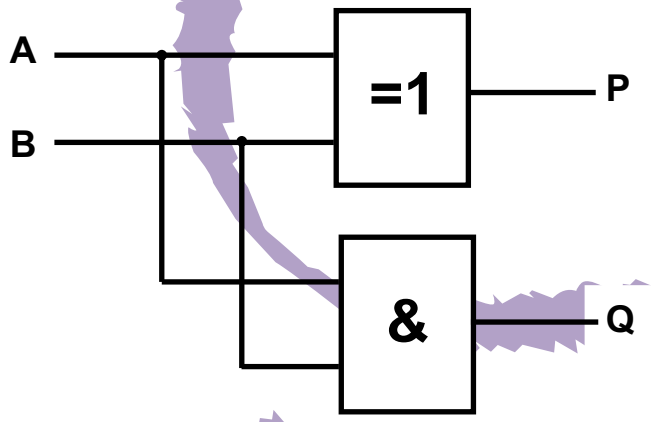

FIGURE 1

1.3.1 What type of arithmetic element is represented by FIGURE 1? (2)

1.3.2 What is the name of the arithmetic element represented by FIGURE 1 above? (1)

1.3.3 Which output of the arithmetic element in FIGURE 1 is represented by the letter P? (1)

1.3.4 Draw the IEC symbol for the logic circuit in FIGURE 1 above. (3)
[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 Standard ASCII codes consist of seven bits, but communications equipment usually sends data in eight-bit (byte) groups. The extra bit is often used as a *parity bit*.

2.1.1 What is the purpose of a parity bit? (2)

2.1.2 How is a parity bit used? (4)

2.2 Explain the difference between *word* and *word length*. (2)

2.3 Determine the decimal equivalent for the following codes:

2.3.1 11011 Gray code

2.3.2 Number 11001010.0111 excess-3

(2 × 3) (6)

2.4 Write the word 'Number' using the ASCII code. (6)
[20]

QUESTION 3: LOGIC GATES, INTERGRATED CIRCUITS AND LOGIC FAMILIES

3.1 Analyse the TWO logic circuits in FIGURE 2 and answer the questions.

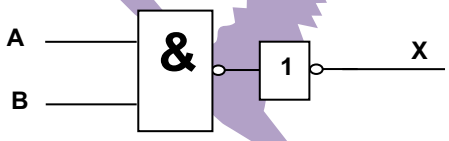

FIGURE 2(a)

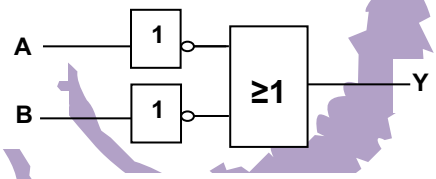

FIGURE 2(b)

3.1.1 Draw the truth-table for FIGURE 2(a) and FIGURE 2(b) above. (6)

3.1.2 What is the relationship between output X and output Y above? (2)

3.1.3 Identify the name(s) of gate(s) represented by the logic circuit in the figures above. (2)

3.2 Draw the circuit diagram for a TWO-input ECL OR gate. (5)

3.3 Draw the switch circuit for an XOR gate. (3)

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3.4 What is the meaning of the following abbreviations?

3.4.1 SSI

3.4.2 ECL

(2 × 1) (2)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Draw a logic circuit for a clocked JK flip-flop and explain what it does when clocked if J = K = 0; J = K = 1 and J = 1, K = 0. (8)

4.2 Draw the corresponding output waveform Q for a positive edge-triggered S-R flip-flop with inputs as shown in FIGURE 3 below. Assume Q starts LOW.

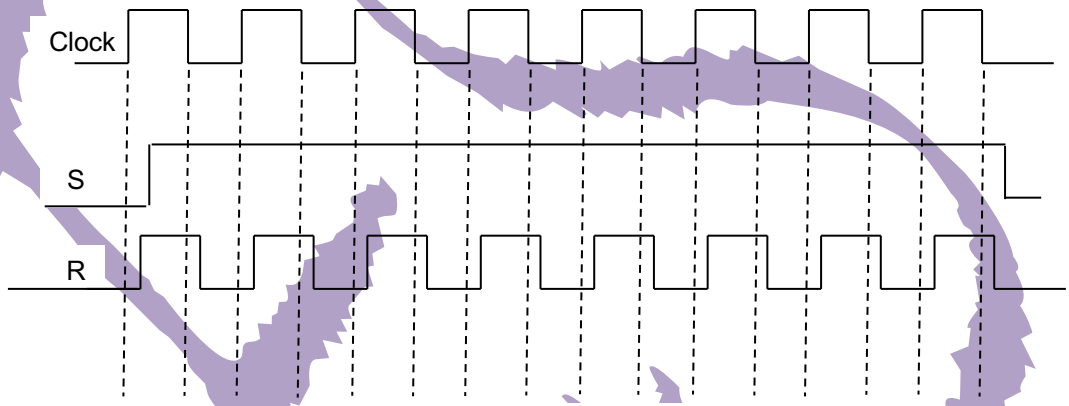

FIGURE 3

(4)

4.3 Suppose your memory card has a capacity of 4GB, how much data expressed in megabytes (MB) can it store? (2)

4.4 Group the following memories as either MAIN or AUXILIARY memories:

semiconductor; magnetic drum; flash disk; hard-drive; CD-ROM; magnetic core (6)
[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1. Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (5.1.1–5.1.6) in the ANSWER BOOK.

5.1.1 Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counters because the …

A input clock pulses are applied only to the first and last stages.
B input clock pulses are applied only to the last stage.
C input clock pulses are not used to activate any of the counter stages.
D input clock pulses are applied simultaneously to each stage.

5.1.2 Mod-6 and mod-12 counters are most commonly used in …

A frequency counters.
B power consumption meters.
C digital clocks.
D multiplexed displays.

5.1.3 What is a shift register called which will accept a parallel input and can shift data left or right?

A Tristate
B End-around
C Bidirectional universal
D Conversion

5.1.4 Which type of counter circuit may easily generate a sequence of equally spaced timing pulses?

A Clock
B Shift register sequencer
C Johnson
D Binary

5.1.5 What is meant by parallel-loading the register?

A Loading data in all four flip-flops at the same time
B Momentarily disabling the synchronous SET and RESET inputs
C Loading data in two of the flip-flops
D Shifting the data in all flip-flops simultaneously

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5.1.6 One of the major drawbacks of the use of asynchronous counters is that …

A low-frequency applications are limited because of internal propagation delays.
B high-frequency applications are limited because of internal propagation delays.
C asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications.
D asynchronous counters do not have propagation delays, which limits their use in high-frequency applications.

(6 × 1) (6)

5.2 Draw the timing diagram for modulo 5 DOWN counter. (4)

5.3 Draw a neatly labelled sketch of a 4-bit LEFT-RIGHT shift register using D-type flip-flops and show all the inputs and outputs. (10)
[20]

TOTAL: 100

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