201304T187

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Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T940(E)(M26)T
APRIL EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

26 March 2013 (X-Paper)
09:00–12:00

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

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SECTION A

QUESTION 1

1.1 Various options are given as possible answers for the following questions. Choose the correct answer and write only the letter (A–D) next to the question number (1.1.1–1.1.10) in the ANSWER BOOK.

1.1.1 A full adder can be made up of ...

A two half adders.
B two half adders and a NOR gate.
C two half adders and an OR gate.
D two half adders and an AND gate.

1.1.2 The number FF in the hexadecimal system is equivalent to ... in the decimal system.

A 256
B 255
C 240
D 239

1.1.3 How many bits are there in an ASCII character?

A 16
B 8
C 7
D 4

1.1.4 A parity bit is ...

A used to indicate uppercase letters.
B used to detect errors.
C is the first bit in a byte.
D is the last bit in a byte.

1.1.5 What is the output state of an OR gate if the inputs are 0 and 1?

A 0
B 1
C 3
D 2

1.1.6 In standard TTL logic, the 'totem pole' stage refers to ...

A the multi-emitter input stage.
B the output buffer.
C the phase-splitter.
D open-collector output stage

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1.1.7 Semiconductor memories are preferred because they are …

A volatile and of small size.
B nonvolatile and of large size.
C nonvolatile and of small size.
D easily magnetisable.

1.1.8 In a JK flip-flop toggle means …

A to set Q = 1 and Q'= 0.
B to set Q = 0 and Q'= 1.
C to change the output to the opposite state.
D that there is no change in the input.

1.1.9 A 3-bit up-down counter can count from …

A 000 to 111.
B 111 to 000.
C 000 to 111 and also from 111 to 000.
D 000 to 1000.

1.1.10 Which of the following data sequence is not characteristic of a shift register?

A Serial in parallel in
B Serial in parallel out
C Parallel in serial out
D Parallel in parallel out

(10 × 1) (10)

1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.10) in the ANSWER BOOK.

1.2.1 The MOD number of a Johnson counter will always be equal to one and half the number of flip-flops in the counter.

1.2.2 A parallel counter is also known as a synchronous counter.

1.2.3 Bidirectional shift registers can shift data either right or left.

1.2.4 A parallel-in/serial-out shift register enters all data bits simultaneously and transfers them out one bit at a time.

1.2.5 A full adder adds three bits, a half adder adds one and half bits.

1.2.6 If you borrow from a position that contains a 0, you must borrow from the more significant bit that contains a 1. All 0s up to that point become 1s, and the digit last borrowed from becomes a 0.

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1.2.7 ROM stands for read-write-memory.

1.2.8 Edge-triggered flip-flops can be identified by the triangle on the clock input.

1.2.9 ASCII codes are used strictly for representing letters, digits, etc.

1.2.10 The most significant digit is the rightmost, largest-weight digit in a number.

(10 × 1) (10)

1.3 Choose an item/word from COLUMN B that matches a description in COLUMN A. Write only the letter (A–E) next to the question number (1.3.1–1.3.5) in the ANSWER BOOK.

COLUMN A		COLUMN B	
1.3.1	These codes obey the principle of positional weighting	A	Self-complementing codes
1.3.2	These codes are used to encode the letters of the alphabet, decimal numbers and symbols	B	Non-weighted binary codes
		C	Weighted binary codes
1.3.3	These codes have the property that the 9s complement of a decimal number is obtained directly by taking the 1s complement (changing 1s to 0s and 0s to 1s) of the corresponding number in the code	D	Alphanumeric codes
		E	Hamming code
1.3.4	These codes do not obey the position-weighting principle		
1.3.5	A code that can be used to detect and correct bit errors that can occur when computer data is moved or stored		

(5 × 1) (5)

TOTAL SECTION A: 25

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SECTION B

QUESTION 2

2.1 Briefly explain the difference between a *half adder* and a *full adder*. (4)

2.2 When parity is in use on a computer system, one parity bit is stored in a DRAM along with every 8 bits (1 byte) of data.

2.2.1 Give TWO types of parities that are used on the computer system. (2)

2.2.2 Briefly explain how the two parity types in QUESTION 2.2.1 work. (4)

2.3 State the THREE advantages of using BCD codes. (3)

2.4 Use two's complement to subtract 60_8 from 11001111_2, and then convert the answer to the decimal number system. (4)

2.5 Convert each of the following numbers to its BINARY equivalent and then complete the calculations in the binary number system:

2.5.1 $F_{16} \times 1010_2$ (3)

2.5.2 $226_8 \div 1010_2$ (convert your answer to octal) (4)

2.6 Redraw the following TABLE in the ANSWER BOOK and complete it by making use of the codes indicated on the TABLE. Show ALL the calculations in your ANSWER BOOK.

Binary string	BCD	Excess-three code
100010010111	2.6.1 ...	2.6.2 ...

(3 × 2) (6)
[30]

QUESTION 3

3.1 Definition: The output of gate Y will be logic 1 only if any of the inputs is logic 0, otherwise it will be logic 0.

3.1.1 What is the name of the gate that is defined above? (2)

3.1.2 Draw the IEC symbol of the gate in QUESTION 3.1.1 above. (3)

3.1.3 Draw the truth table for the above gate. (3)

3.2 Give TWO types of integrated circuits (ICs) (2)

3.3 Draw a circuit diagram of a two-input ECL-OR gate. (5)
[15]

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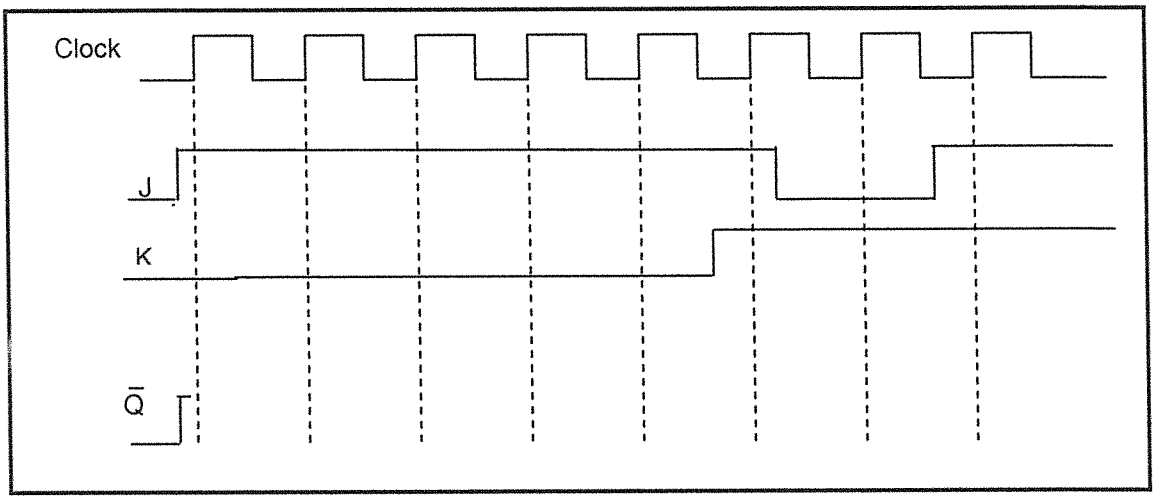
QUESTION 4

4.1 Show how a clocked JK flip-flop can be constructed using NAND gates only. (4)

4.2 Redraw and complete the following timing diagram in the ANSWER BOOK:



TIMING DIAGRAM (4)

4.3 One common type of memory that is used in PCs is called read-only memory (ROM).

4.3.1 Give TWO main reasons why ROM is used in a PC. (2)

4.3.2 List THREE different types of ROMs. (3)

4.4 Why are RAMs called volatile memories? (2)
[15]

QUESTION 5

5.1 What is the difference between a register and a shift register? (4)

5.2 Why are asynchronous counters also called series counters? (2)

5.3 Name FOUR types of shift registers. (4)

5.4 Draw a neat, labelled diagram of a three-bit binary up-counter using JK flip-flops which triggers on a negative edge clock transition. (5)
[15]

TOTAL SECTION B: 75
GRAND TOTAL: 100

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