higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N3

26 MARCH 2013

This marking guideline consists of 7 pages.

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SECTION A

QUESTION 1

1.1	1.1.1	C ✓		
	1.1.2	B ✓		
	1.1.3	C ✓		
	1.1.4	B ✓		
	1.1.5	B ✓		
	1.1.6	B ✓		
	1.1.7	A ✓		
	1.1.8	C ✓		
	1.1.9	C ✓		
	1.1.10	A ✓	(10 × 1)	(10)
1.2	1.2.1	False✓		
	1.2.2	True✓		
	1.2.3	True✓		
	1.2.4	True✓		
	1.2.5	False✓		
	1.2.6	True✓		
	1.2.7	False✓		
	1.2.8	True✓		
	1.2.9	False✓		
	1.2.10	False✓	(10 × 1)	(10)
1.3	1.3.1	C ✓		
	1.3.2	D ✓		
	1.3.3	A ✓		
	1.3.4	B ✓		
	1.3.5	E ✓	(5 × 1)	(5)
				[25]

TOTAL SECTION A: 25

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SECTION B

QUESTION 2

2.1 A half adder is an arithmetic element that performs the addition of two bits, ✓✓ while a full adder is an arithmetic element that performs the addition of three bits. ✓✓ (4)

2.2 2.2.1 Even parity ✓
Odd/Uneven parity✓ (2)

2.2.2 When using even parity, the parity bit is set to 1 if the number of ones in a given set of bits is odd, making the number of ones in the entire set of bits even. ✓ If the number of ones in a given set of bits is already even, it is set to a 0.✓

When using odd parity, the parity bit is set to 1 if the number of ones in a given set of bits is even, keeping the number of ones in the entire set of bits odd. ✓ And when the number of set bits is already odd, the odd parity bit is set to 0.✓ (4)

2.3
- Any large decimal number can be easily converted into corresponding binary number✓
- A person needs to remember only the binary equivalents of decimal numbers from 0 to 9 ✓
- Conversion from BCD into decimal is also very easy ✓ (3)

2.4 $11001111_2 - 60_8$

6	0
110	000

$\therefore 60_8 = 110000_2$✓

2's complement of 00110000 = 11001111 + 1 = 11010000 ✓

```
  1
  0 * 1 1 0 0 1 1 1 1
  1 * 1 1 0 1 0 0 0 0
1 0 * 1 0 0 1 1 1 1 1   ✓
↳ Ignore carry
```

128	64	32	16	8	4	2	1
1	0	0	1	1	1	1	1

$\therefore$ 1001 1111 = 128 + 16 + 8 + 4 + 2 + 1 = 159_{10}✓ (4)

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2.5 2.5.1 $F_{16} \times 1010_2$

$\therefore F_{16} = 1111_2$ ✓

```
                                1   1   1   1
                                1   0   1   0
                                0   0   0   0
                        1       1   1   1
                0       0       0   0       ✓
        1       1       1       1
1       0       0       1       0   1   1   0✓
```

(3)

2.5.2 $226_8 \div 1010_2$

2	2	6
010	010	110

$\therefore 226_8 = 10010110_2$ ✓

```
                                1   1   1   1   ✓
1   0   1   0 | 1   0   0   1   0   1   1   0
                    1   0   1   0
                    1   0   0   0   1
                        1   0   1   0       ✓
                        0   1   1   1   1
                            1   0   1   0   0
                            0   1   0   1   0
                                1   0   1   0
                                        0
```

8	4	2	1
1	1	1	1

$\therefore 1111_2 = 17_8$ ✓

(4)

2.6

Binary string	BCD	Excess-three code
100010010111	897✓✓✓	564✓✓✓

(6)
[30]

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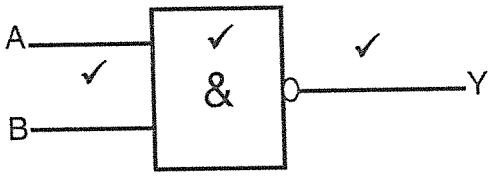
QUESTION 3

3.1 3.1.1 NAND gate ✓✓ (2)

3.1.2



(3)

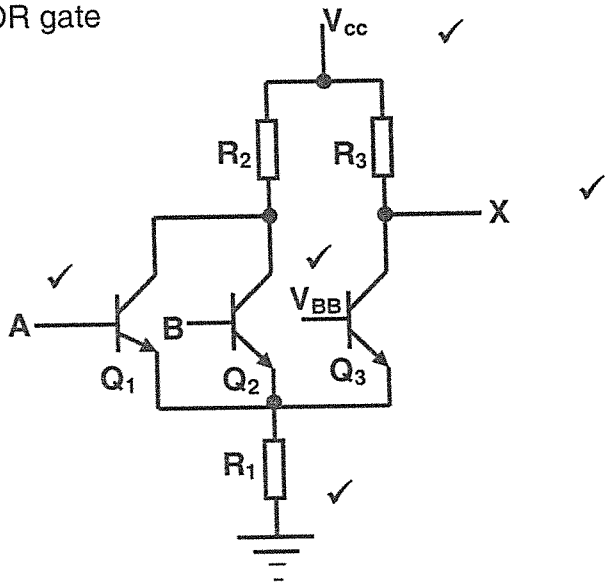
3.1.3

A✓	B✓		Y ✓
0	0		1
0	1		1
1	0		1
1	1		0

(3)

3.2 MOS✓ and Bi-polar✓ (2)

3.4 Two-input ECL-OR gate



(5)
[15]

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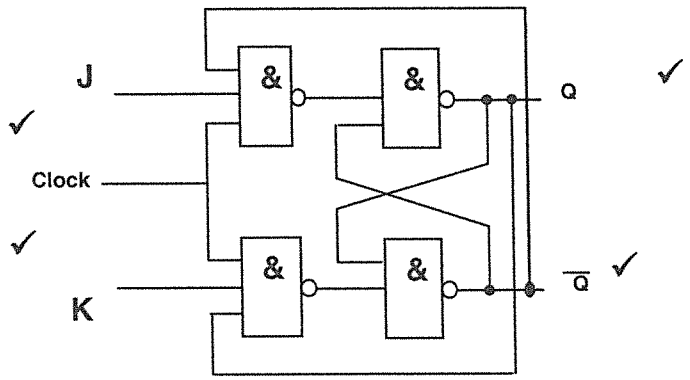
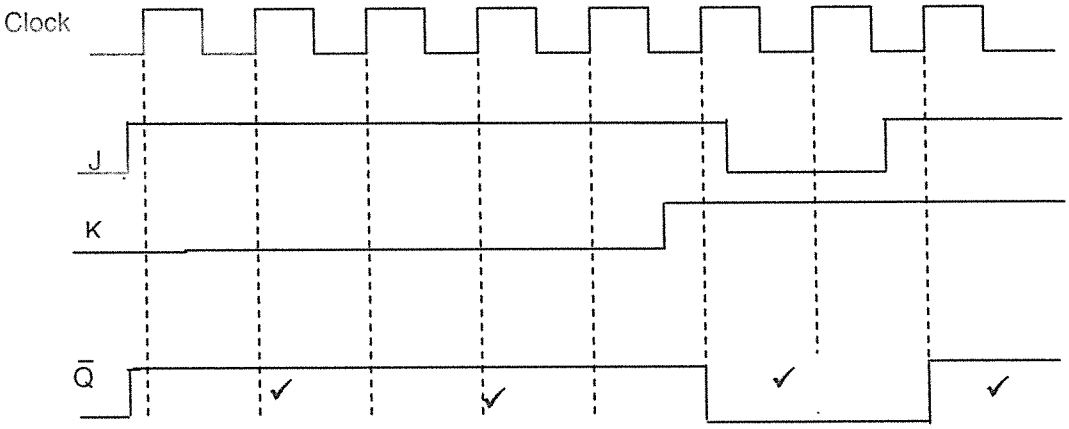
QUESTION 4

4.1



(4)

4.2



(4)

4.3 4.3.1 Permanence✓
Security✓ (2)

4.3.2 PROM✓
EROM✓
EEROM✓ (3)

4.4 RAMs are called volatile memories because RAMs lose stored data when the power is turned off. ✓✓ (2)
[15]

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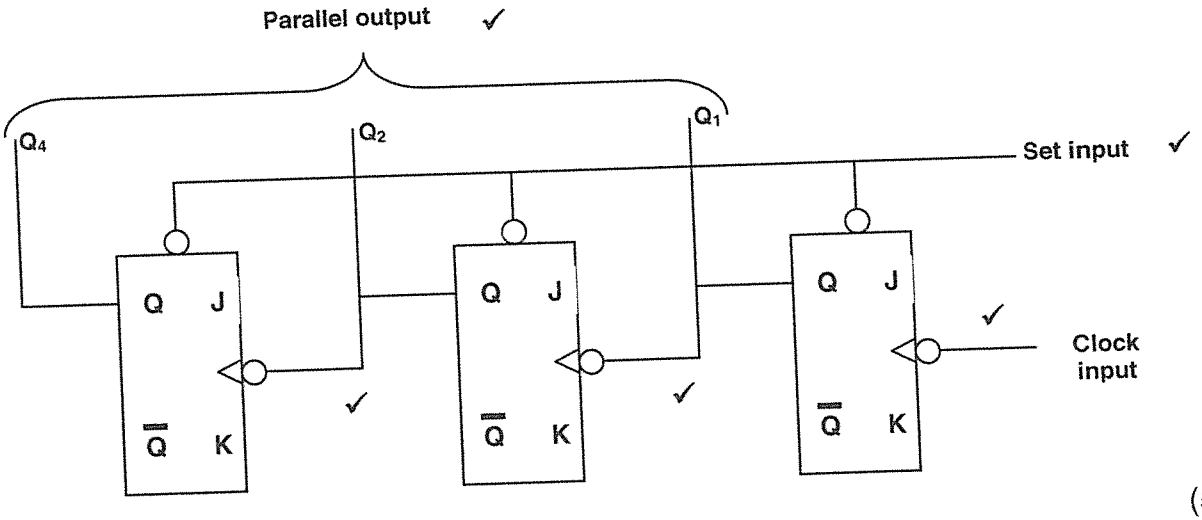
QUESTION 5

5.1 A register is a collection of flip-flops or latches used to store a binary number; it is a one-word memory circuit. ✓✓ A shift register is a register that is used to shift binary words from one direction to another ✓✓ (4)

5.2 Because an output of one flip-flop is a clock of the next one✓✓ (2)

5.3 Serial-in serial-out shift register✓
Serial-in parallel-out shift register✓
Parallel-in serial-out shift register✓
Parallel-in parallel-out shift register✓
Bidirectional shift register (4)

5.4



(5)
[15]

TOTAL SECTION B: 75
GRAND TOTAL: 100

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