higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T930**(E)**(A6)T

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

6 August 2019 (X-Paper)
09:00–12:00

Calculators may NOT be used.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Keep questions and subsections of questions together.
5. Show ALL the steps and calculations.
6. ALL the sketches and diagrams must be large, clear and neat.
7. Write neatly and legibly.

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QUESTION 1: NUMBER SYSTEMS

Convert each of the numbers below to their binary equivalents, where applicable, then complete the calculations in the binary number system and then follow the instruction given. Show ALL conversions.

1.1 $10111,10_2 + 2,75_{10} + 3,6_8$

Convert the final answer to the hexa-decimal number system.

1.2 $15,5_{10} \times 1,2_8$

Convert the final answer to the octal number system.

1.3 $A,B5_{16} - 3,6_8$

Use the complement and convert the final answer to the octal number system.

1.4 $60,4_{16} \div 3,4_8$

Convert the final answer to the decimal number system.

(4 × 5) **[20]**

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS, DECODERS AND ARITHMETIC ELEMENTS

2.1 Complete the paragraph below by writing the missing word next to the question number (2.1.1–2.1.5) in the ANSWER BOOK.

A full adder is constructed from two (2.1.1) … adders and an (2.1.2) … gate. The full adder can add up to (2.1.3) … bits, giving an output as a/an (2.1.4) … and a/an (2.1.5) … (5)

2.2 Clarify the acronym EBCDIC. (2)

2.3 Encode the following to the EBCDIC code:

J a k e 2 (5)

2.4 Encode or decode the following numbers to the equivalent asked:

2.4.1 $8\bar{4}\bar{2}\bar{1}_{\text{ BCD code}}$ 100101011010 to its decimal equivalent

2.4.2 128_{10} to Gray code

(2 × 3) (6)

2.5 Define *parity bit* and explain why it is used. (2)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'True' or 'False' next to the question number (3.1.1–3.1.5) in the ANSWER BOOK.

3.1.1 As a rule CMOS has the lowest power consumption of all IC families.

3.1.2 An exclusive OR gate output is HIGH when the inputs are unequal.

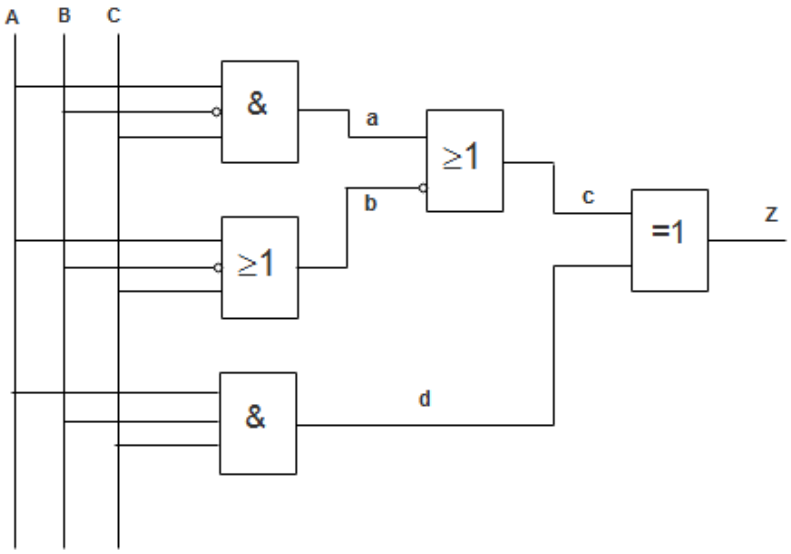
3.1.3 A NOR gate output is LOW if any of its inputs is LOW.

3.1.4 A truth table illustrates how the input level of a gate responds to all the possible output level combinations.

3.1.5 A waveform can be enabled or disabled by both AND and OR gates.

(5 × 1) (5)

3.2 The circuit diagram below consists of AND gates, OR gates and an XOR gate.



Copy the truth table for the circuit and complete it in the ANSWER BOOK.

A	B	C	a	b	c	d	Z
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

(5)

3.3 Draw a neat, labelled circuit diagram for the Boolean expression below without changing or simplifying the expression.

$$Z = A\bar{B}C + \overline{A\bar{C} + AB}$$ (5)

3.4 Draw a neat labelled circuit diagram for a TTL NAND gate with a totem pole connected output. (5)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

4.1.1 The number of 16 k × 4 memories needed to construct a 128 k × 8 memory is …

A 4.
B 8.
C 12.
D 16.

4.1.2 Because of their non-volatility, high speed, low power requirements, and lack of moving parts … have become feasible alternatives to magnetic disk storage.

A CD-ROMs
B flash memory modules
C ROMs
D EPROMs

4.1.3 The memory operation that stores data into a memory location after entering a new address is called …

A a read cycle.
B a write cycle.
C a refresh cycle.
D chip select.

4.1.4 When a computer is executing a program of instructions the CPU will … memory locations as dictated by the programme instructions.

A format
B scan
C store data into
D verify

4.1.5 Information that is stored in a mask ROM …

A can be modified by using special equipment.
B is stored by the manufacturer and cannot be changed.
C is lost if power is interrupted.
D can be modified by using special equipment and is lost if power is interrupted.

(5 × 1) (5)

4.2 Clarify the following acronyms

4.2.1 RAM

4.2.2 ROM

4.2.3 DVD-RW

4.2.4 PROM

4.2.5 EEPROM

(5 × 1) (5)

4.3 Draw a neat, labelled circuit diagram of a master/slave flip-flop that uses JK flip-flops. (10) **[20]**

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'True' or 'False' next to the question number (3.1.1–3.1.5) in the ANSWER BOOK.

5.1.1 A ripple counter is a synchronous counter.

5.1.2 *Bi-directional* means having two states.

5.1.3 In many cases counters must be strobed in order to eliminate glitches.

5.1.4 The MOD number of a Johnson counter will always be equal to one-half the number of flip-flops in the counter.

5.1.5 An asynchronous counter differs from a synchronous counter in the clocking method.

(5 × 1) (5)

5.2 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (5.2.1–5.2.5) in the ANSWER BOOK.

5.2.1 Many parallel counters use … pre-setting whereby the counter is pre-set on the active transition of the same clock signal that is used for counting.

A feedback
B synchronous
C ripple
D asynchronous

5.2.2 In order to use a shift register as a counter …

A the register's serial input is the counter input and the serial output is the counter output
B the parallel inputs provide the input signal and the output signal is taken from the serial data output
C serial in/serial out register must be used
D the serial output of the register is connected back to the serial input of the register

5.2.3 The MOD-10 counter is also referred to as a … counter.

A decade
B strobing
C BCD
D circuit

5.2.4 A J-K flip-flop is reset and must stay reset after the clock pulse. This transition requires that …

A J and K inputs must both be 0.
B J must be 0, K doesn't matter.
C J doesn't matter, K must be 0.
D J must be 0 and K must be 1.

5.2.5 A BCD counter has … states.

A 8
B 9
C 10
D 11

(5 × 1) (5)

5.3 The table below shows a number of clock pulses and the output per clock pulse.

Clock pulses	Q8	Q4	Q2	Q1
0	1	1	0	1
1	1	0	0	0
2	0	0	0	0
3	0	0	0	1
4	0	0	1	1
5	0	1	1	1
6	1	1	1	1
7	1	1	1	0
8	1	1	0	0
9	1	0	0	0
10	0	0	0	0
11	0	0	0	1

5.3.1 Draw the timing diagram for the table above. Show ALL clock pulses. (6)

5.3.2 Does the table represent a counter or a shift register? (2)

5.3.3 Give the name of the counter or shift register indicated in QUESTION 5.3.2. (2)

[20]

TOTAL: 100

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