higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

16 April 2021

This marking guideline consists of 7 pages.

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QUESTION 1: NUMBER SYSTEMS

1.1 $FA,2_{16} + 7,6_8 + 1111,1011_2$

$FA,2_{16} = 11111010,0010_2$ √

$7,6_8 = 111,110_2$ √

$$\begin{array}{r} 11111010,0010 \\ 00000111,1100 \\ +\ 00001111,1011 \\ \hline 100010001,1001 \end{array}$$ √ √ ✓

$100010001,1001_2 = 111,9_{16}$ ✓

(4)

1.2 $34,1_8 \times 12,5_{10}$

$34,1_8 = 011100,001_2$ √

$12,5_{10} = 1100,1_2$ √

$$\begin{array}{r} 11100,001 \\ \times\ 1100,100 \\ \hline 1110000100 \\ 1110000100000 \\ +\ 11100001000000 \\ \hline 101011111,100100 \end{array}$$ ✓ ✓ ✓

$101011111,100100_2 = 537,44_8$ ✓

(5)

1.3 $26,6_8 = 010110,110_2$ √

$1A,C_{16} = 00011010,1100_2$ · √

$$\begin{array}{rl} 10110,1100 & \longrightarrow \quad 10110,1100 \\ -\ 11010,1100 & \longrightarrow \quad 00101,0011 \text{ (1's c)} \\ & \qquad\qquad\quad +1 \\ & \qquad\qquad\quad 00101,0100 \text{ (2's c)} \checkmark \end{array}$$

$$\begin{array}{r} 10110,1100 \\ +\ 00101,0100 \\ \hline 11100,0000 \checkmark \end{array}$$

$$\begin{array}{r} 00011,1111 \\ +1 \\ \hline -\ 00100,0000 \checkmark \end{array}$$

$-\ 100_2 = -\ 4_{10}$ ✓ (5)

1.4 $4B,6_{16} \div 4,5_{10}$

$4B,6_{16} = 01001011,0110_2$ · √

$4,5_{10} = 100,1_2$ · √

$$\begin{array}{r} 10000,11 \checkmark \\ 1001\overline{)10010110,110} \\ \underline{-1001} \checkmark \\ 01101 \\ \underline{-1001} \checkmark \\ 1001 \\ \underline{-1001} \checkmark \end{array}$$

$10000,11_2 = 16,75_{10}$ ✓

(6)
[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS, DECODERS AND ARITHMETIC ELEMENTS

2.1 Extended Binary Coded Decimal Interchange Code (2)

2.2
E 1100 0101✓
q 1001 1000✓
M 1101 0100✓
c 1000 0011✓
2 1111 0010✓ (5)

2.3 2.3.1 1010 0111 0110
= 6✓ 1✓ 2✓
= 612_{10} (3)

2.3.2 101_{10}
$=1100101_2$✓

$1+1+0+0+1+0+1$ Binary✓
1 0 1 0 1 1 1 Gray✓ (3)

2.4 A 2421 BCD decoder has 10 output lines because it starts decoding from 0000(0) to 1111(9) which means that it decodes 10 times. (2)

2.5

P_1	P_2	D_1	P_3	D_2	D3	D_4	P_4	D_5	D_6
1	2	3	4	5	6	7	8	9	10
?	?	1	?	0	1	0	?	1	1

1,3,5,7,9	P1 + D1 + D2 + D4
	P1 + 1 + 0 + 0 + 1
	P1 = 0 ✓

2,3,6,7,10	P2 + D1 + D3 + D4 + D6
	P2 + 1 + 1 + 0 + 1
	P2 = 1 ✓

4,5,6,7	P3 + D2 + D3 + D4
	P3 + 0 + 1 + 0
	P3 = 1 ✓

8,9,10	P4 + D5 + D6
	P4 + 1 + 1
	P4 = 0 ✓

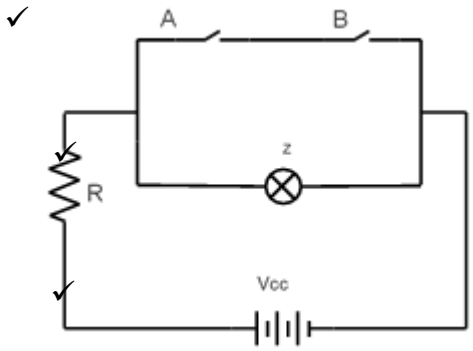
The new word is 0111010011 ✓ (5)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 3.1.1 A
3.1.2 A
3.1.3 C
3.1.4 A
3.1.5 B

(5 × 1) (5)

3.2 3.2.1



(3)

3.2.2

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

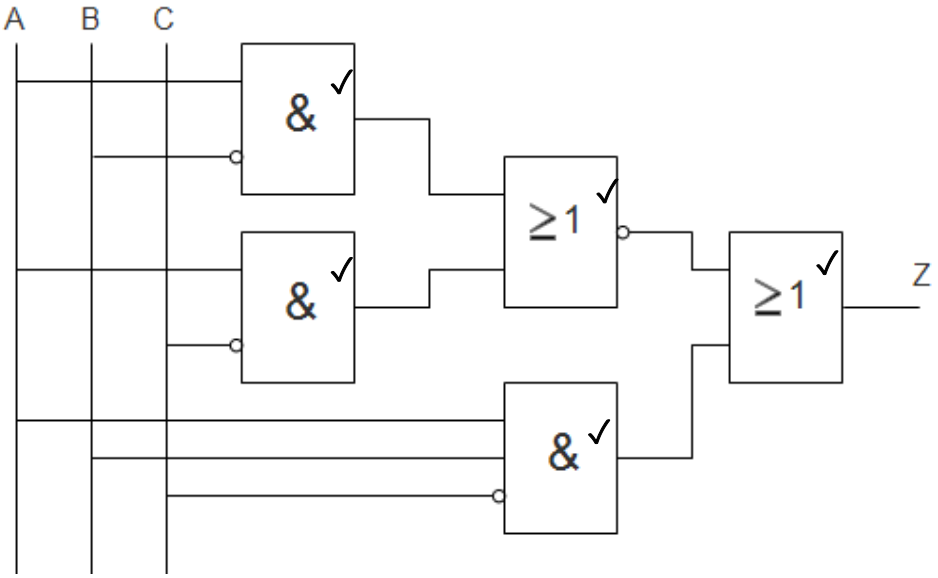
(2)

3.3

A	B	C	a	b	c	d	Z
0	0	0	1	0	1	0	0
0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0
			✓	✓	✓	✓	✓

(5)

3.4



(5)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 4.1.1 Random-access memory
4.1.2 Erasable programmable read-only memory
4.1.3 Programmable read-only memory

(3 × 1) (3)

4.2 4.2.1 J = 1, K = 1
4.2.2 J = 0, K = 0
4.2.3 J = 1, K = 0
4.2.4 J = 0, K = 1

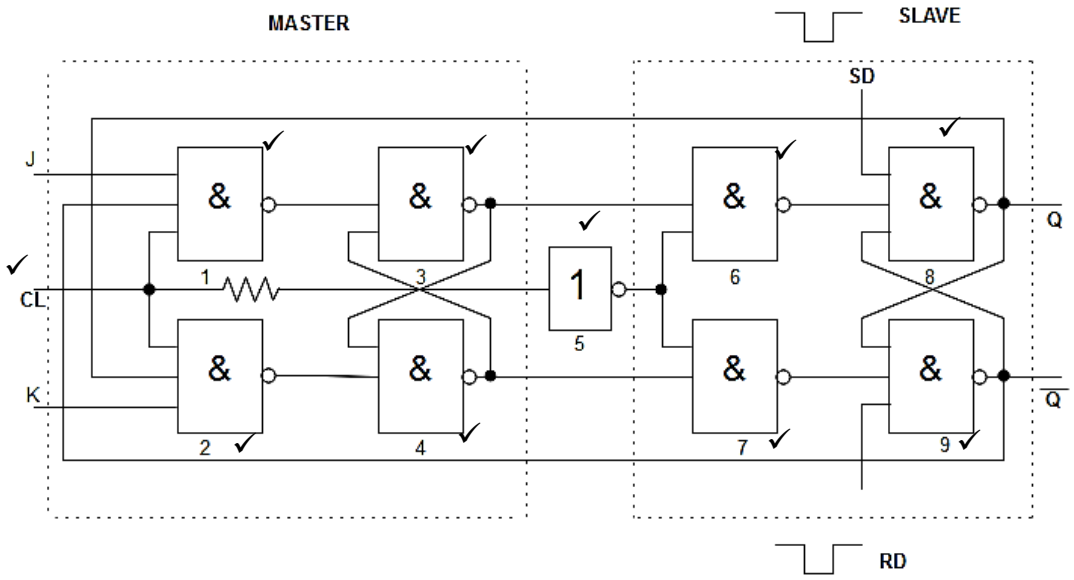
(4 × 1) (4)

4.3 When J = 1 and K = 1 (1)

4.4 SR flip-flop
Clocked SR flip-flop
SR master slave flip-flop

(Any 2×1) (2)

4.5



(10)
[20]

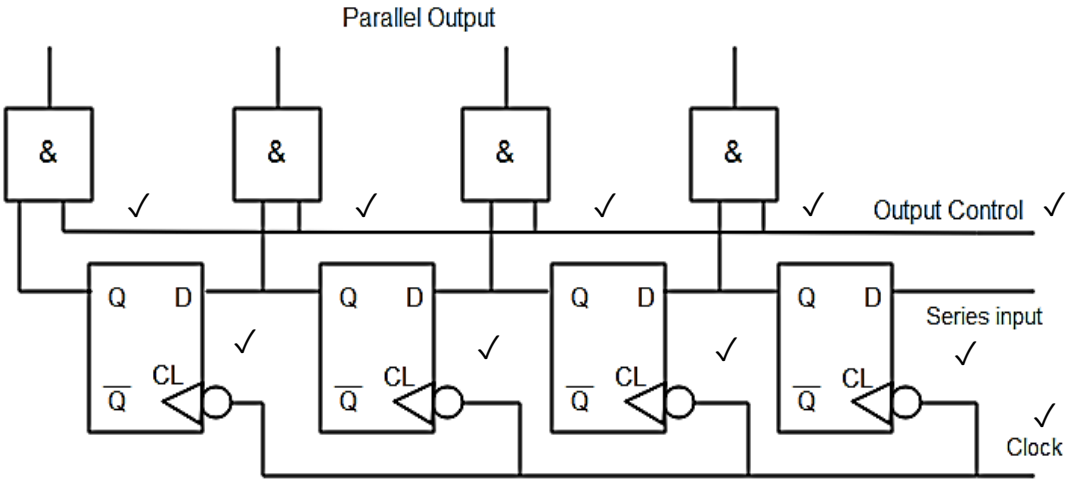
QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1
5.1.1 True
5.1.2 False
5.1.3 False
5.1.4 True
5.1.5 True
5.1.6 True (6 × 1) (6)

5.2 The purpose of a shift register is to store data temporarily or to convert parallel data to serial data and vice versa. (2)

5.3 Module 3 and module 5 counter (2)

5.4



(10)
[20]

TOTAL: 100

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