higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T930**(E)**(A8)T

# NATIONAL CERTIFICATE

# LOGIC SYSTEMS N3

(8080273)

**8 April 2019 (X-Paper)**
**09:00–12:00**

**Calculators may NOT be used.**

**This question paper consists of 10 pages.**

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# DEPARTMENT OF HIGHER EDUCATION AND TRAINING
# REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

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**INSTRUCTIONS AND INFORMATION**

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Keep questions and subsections of questions together.
5. ALL sketches and diagrams must be large, clear and neat.
6. Show ALL steps and calculations.
7. Write neatly and legibly.

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## QUESTION 1: NUMBER SYSTEMS

Convert each of the following numbers to their binary equivalents and then complete the calculations in the binary number system and then follow the instruction given. Show ALL conversions.

1.1 $3,4C_{16} + 7,1_8 + 100,100_2$

Convert the final binary answer to the octal number system.

1.2 $3B,6_{16} \times 3,5_{10}$

Convert the final binary answer to the hexa-decimal number system.

1.3 $32,5_{10} - 3,A_{16}$

Use the two's complement method and convert the final binary answer to the octal number system.

1.4 $40,5_8 \div 4,5_{10}$

Convert the final binary answer to the decimal number system.

(4 × 5) **[20]**

## QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS, DECODERS AND ARITHMETIC ELEMENTS

2.1 Choose a description from COLUMN B that matches a code in COLUMN A. Write only the letter (A–G) next to the question number (2.1.1–2.1.5) in the ANSWER BOOK.

| COLUMN A | | COLUMN A | |
|---|---|---|---|
| 2.1.1 | Excess 3 code | A | Alpha-numeric code where B is represented by 1100 0010 |
| 2.1.2 | EBCDIC code | B | Unweighted nonself-complementing code |
| 2.1.3 | Gray code | C | Self-complementing weighted code |
| 2.1.4 | 2421 BCD code | D | Complementary code |
| 2.1.5 | Hexa-decimal code | E | Self-complementing unweighted code |
| | | F | Weighted code |
| | | G | Code where four bits can be represented by a single symbol |

(5 × 1) (5)

2.2 Clarify the acronym ASCII. (2)

2.3 Encode the following to ASCII code:

**@ R U M !** (5)

2.4 Encode each of the following to the code indicated:

2.4.1 $214_{10}$ to 7421 BCD code

2.4.2 $345_{10}$ to Excess 3 code

(2 × 3) (6)

2.5 Define the concept of *word length* as applicable to data communication. (2)

**[20]**

## QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (3.1.1–3.1.5) in the ANSWER BOOK.

3.1.1 How many inputs of a four-input AND gate must be HIGH for the output of the logic gate to go HIGH?

A Any one of the inputs
B Any two of the inputs
C Any three of the inputs
D All four inputs

3.1.2 Which ONE of the following gates has the exact inverse output of the OR gate for all possible input combinations:

A AND
B NAND
C NOR
D OR

3.1.3 One advantage TTL has over CMOS is that TTL is …

A Less expensive.
B Not sensitive to electrostatic discharge.
C Faster.
D More widely available.

3.1.4 How many input combinations would a truth table for a six-input AND gate have?

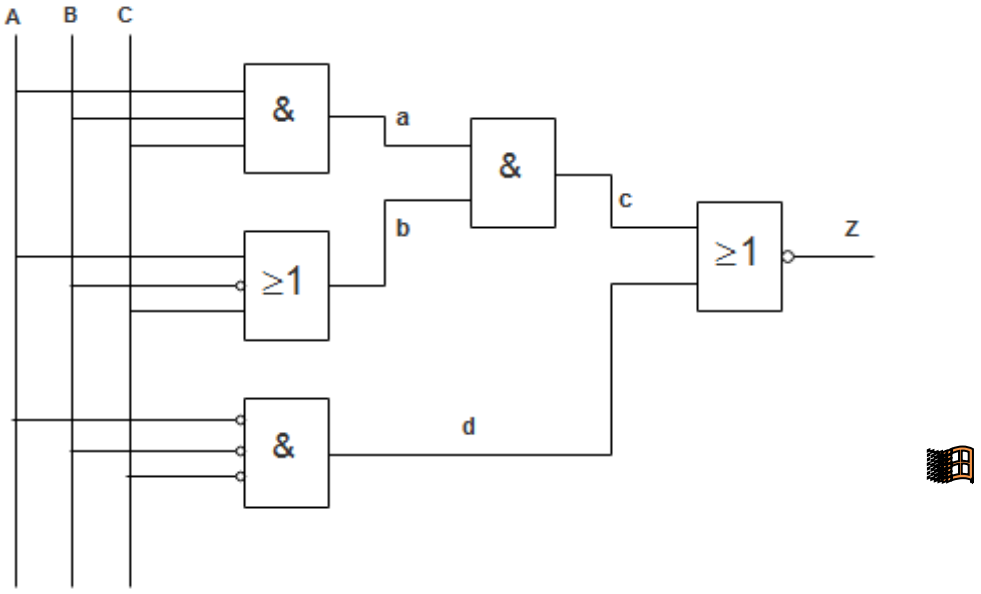
A 32
B 48
C 64
D 128

3.1.5 The terms *low speed* and *high speed*, applied to logic circuits, refer to the …

A Rise time.
B Fall time.
C Propagation delay time.
D Clock speed.

(5 × 1) (5)

3.2 Given below is a circuit diagram that consists of AND gates and OR gates.




Copy and complete the truth table for the circuit.

| A | B | C | a | b | c | d | Z |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | | |
| 0 | 0 | 1 | | | | | |
| 0 | 1 | 0 | | | | | |
| 0 | 1 | 1 | | | | | |
| 1 | 0 | 0 | | | | | |
| 1 | 0 | 1 | | | | | |
| 1 | 1 | 0 | | | | | |
| 1 | 1 | 1 | | | | | |

(5)

3.3 Make a neat, labelled sketch of the circuit diagram of the Boolean expression below without changing or simplifying the expression.

$$Z = (A+B)(A.C) + \bar{A}\bar{B}C$$ (5)

3.4 A TTL-NAND gate is implemented by using transistor-transistor logic.

Draw the circuit diagram for an open-collector TTL-NAND gate. (5)
**[20]**

## QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

4.1.1 Information stored in an EEPROM …

A can be modified by performing a memory-write operation.
B is stored by the manufacturer and cannot be changed.
C is lost if power is interrupted.
D can be erased by applying high voltage to each storage location.

4.1.2 The difference between RAM and ROM is that …

A RAM has a read/write signal and ROM does not.
B RAM will lose data when the power is removed and ROM will not.
C RAM has random address access and ROM uses sequential address access.
D Both A and B.

4.1.3 The major advantage of dynamic RAM over static RAM is …

A cost and storage density.
B cost.
C speed.
D storage density.

4.1.4 The memory operation that presents data on the memory outputs after entering a new address is called a …

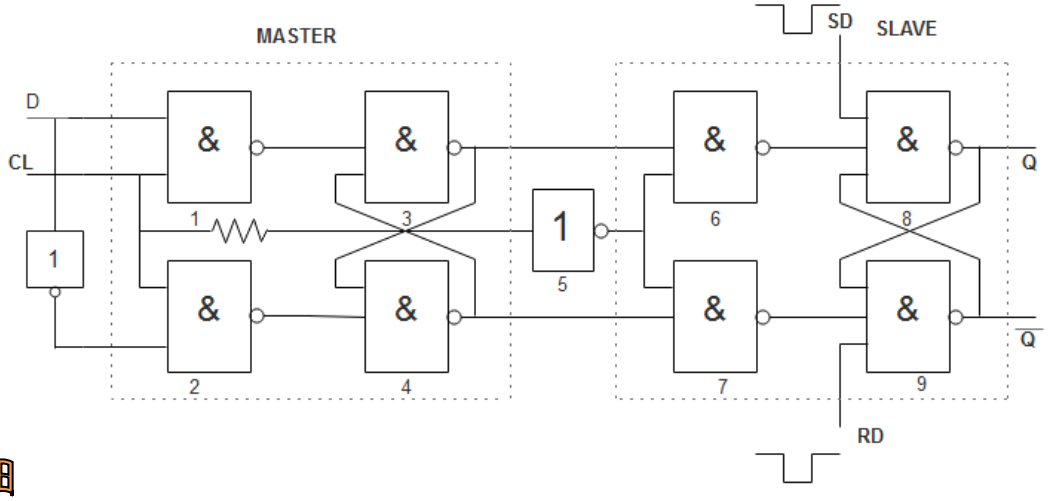
A write cycle.
B read cycle.
C refresh cycle.
D chip select.

4.1.5 Dynamic memory is memory …

A that will maintain storage even if power is removed.
B of which data can never be altered.
C that must be refreshed periodically or it will lose storage.
D that maintains storage as long as power is applied.

(5 × 1) (5)

4.2 Given below is a D-type master-slave flip-flop.




4.2.1 Why is the D-type master-slave flip-flop also known as a *delay flip-flop*? (2)

4.2.2 Draw the truth table for the D-type master-slave flip-flop. (2)

4.2.3 Give the name of the gate used at Point 5. (1)

4.2.4 What is the role of the gate mentioned in QUESTION 4.2.3? (2)

4.3 Write each of the following acronyms in full and give a brief description of each memory-storage device:

4.3.1 DVD-R

4.3.2 CD-RW

(2 × 2) (4)

4.4 Complete the following paragraph by writing the missing words next to the question number (4.4.1–4.4.4) in the ANSWER BOOK.

The clocked RS flip-flop changes on a (4.4.1) … clock pulse. It is made from four (4.4.2) … gates. The disadvantage of the RS flip-flop is that the outcome is (4.4.3) … if two logic (4.4.4) … are applied to the R or S and the S or R inputs.

(4 × 1) (4)

**[20]**

## QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'True' or 'False' next to the question number (5.1.1–5.1.5) in the ANSWER BOOK.

5.1.1 Ring and Johnson shift counters are uncommon circuits similar to synchronous counters.

5.1.2 A universal shift register has both serial and parallel input and output capacity.

5.1.3 The storage capacity of a register makes it an important type of memory.

5.1.4 To transmit parallel data over a serial cable, the data must first go through data conversion to the serial format.

5.1.5 There are eight states in an 8-bit Johnson counter sequence.

(5 × 1) (5)

5.2 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (5.2.1–5.2.5) in the ANSWER BOOK.

5.2.1 Which segments (by letter) of a seven-segment display must be active to display the digit 6?

A b, c, d, e, f, and g
B a, c, d, e, f, and g
C a, b, c, d, and f
D b, c, d, e, and f

5.2.2 Which ONE of the following groups of logic devices would be the minimum required for a MOD-64 synchronous counter:

A Five flip-flops, three AND gates
B Seven flip-flops, five AND gates
C Four flip-flops, ten AND gates
D Six flip-flops, four AND gates

5.2.3 Which ONE of the following statements best describes the operation of a synchronous up-/down-counter?

A The counter can count in either direction, but must continue in that direction once started.
B The counter can be reversed, but must be reset before counting in the other direction.
C In general, the counter can be reversed at any point in its counting sequence.
D The count sequence cannot be reversed, once it has begun, without first resetting the counter to zero.

5.2.4 The parallel outputs of a counter circuit represent the …

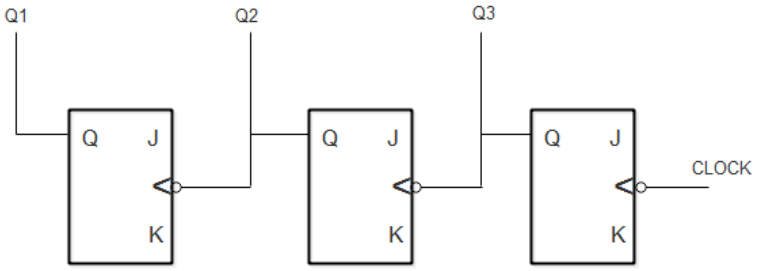
A parallel data word.
B clock frequency.
C counter modulus.
D clock count.

5.2.5 How many natural states will there be in a 4-bit ripple counter?

A 16
B 8
C 4
D 32

(5 × 1) (5)

5.3 The circuit below represents a counter.




5.3.1 What is the highest number (in binary) that this counter can count to? (2)

5.3.2 Draw the truth table that represents the counting sequence of the above counter. (4)

5.4 What is the difference between the *rising time* and the *falling time* with reference to a clock wave? (2 × 2) (4)

**[20]**

**TOTAL: 100**

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