higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

6 APRIL 2018

This marking guideline consists of 7 pages.

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✓ = 1 mark √ ½ mark

QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

1.1 $4A,6_{16} + 3,7_8 + 5,25_{10}$

$4A, 6_{16} = 1\ 0\ 0\ 1\ 0\ 1\ 0, 0\ 1\ 1_2$ √
$3, 7_8 = 1\ 1. 1\ 1\ 1_2$ √
$5, 25_{10} = 1\ 0\ 1, 0\ 1\ 0_2$ ✓

1	0	0	1	0	1	0	,	0	1	1		
					1	1	,	1	1	1		
				1	0	1	,	0	1	0	+	✓
1	0	1	0	0	1	1	,	1	0	0		✓

$1\ 0\ 1\ 0\ 0\ 1\ 1, 1\ 0\ 0_2 = 53,8_{16}$ ✓ (5)

1.2 $A,B7_{16} - 3,2_8$

$A,B7_{16} = 1\ 0\ 1\ 0, 1\ 0\ 1\ 1\ 0\ 1\ 1\ 1_2$ √
$3,2_8 = 0\ 0\ 1\ 1, 0\ 1\ 0\ 0\ 0\ 0\ 0\ 0_2$ √

	1	0	1	0	,	1	0	1	1	0	1	1	1		
1c	1	1	0	0	,	1	0	1	1	1	1	1	1	+	✓
1	0	1	1	1	,	0	1	1	1	0	1	1	0		
													1	+	
	0	1	1	1	,	0	1	1	1	0	1	1	1		✓

$1\ 1\ 1, 0\ 1\ 1\ 1\ 0\ 1\ 1\ 1_2 = 7, 356_8$ ✓

(5)

1.3 $110,5_{10} \times 1,2_8$

$110,5_{10} = 1\ 1\ 0\ 1\ 1\ 1\ 0, 1_2$ √
$1,2_8 = 1, 0\ 1\ 0_2$ √

				1	1	0	1	1	1	0	,	1	0	0		
										1	,	0	1	0	×	
	1	1	0	1	1	1	0	1	0	0	,	0	0	0		✓
			1	1	0	1	1	1	0	1		0	0		+	✓
1	0	0	0	1	0	1	0	0	0	1	,	0	0	0		✓

$1\ 0\ 0\ 0\ 1\ 0\ 1\ 0, 0\ 0\ 1\ 0\ 0\ 0_2 = 8A, 2_{16}$ ✓

(5)

1.4 $86{,}2_{16} \div 7{,}25_{10}$

$86{,}2_{16} = 1\ 0\ 0\ 0\ 0\ 1\ 1\ 0,\ 0\ 0\ 1\ 0_2$ √
$7{,}25_{10} = 1\ 1\ 1,\ 0\ 1_2$ √

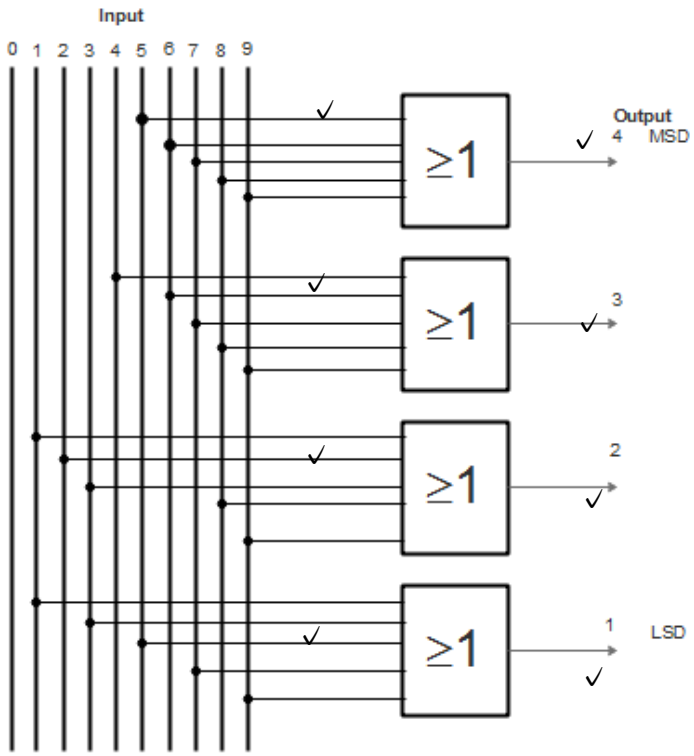
```
                                  1  0  0  1  0  ,  1  ✓
 1  1  1  0  1 | 1  0  0  0  0  1  1  0  0  0  ,  1  0
                 -  1  1  1  0  1
                          1  0  0  0  0  0
                       -     1  1  1  0  1  ✓
                                  1  1  1  0  ,  1
                                -  1  1  1  0     1  ✓
                                  0  0  0  0  ,  0
```

$1\ 0\ 0\ 1\ 0,\ 1_2 = 4,\ 625_{10}$ ✓

(5)
[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1



(8)

2.2 2.2.1 $1\ 0\ 0\ 1\ 1\ 1\ 0\ 1\ 1\ 1\ 0\ 0_{2421BCD}$
$= 3\ \ 7\ \ 6_{10}$

2.2.2 425_{10}
Binary = 1 0 0 0 0 1 0 0 1 0 1
Gray = 1 1 0 0 0 1 1 0 1 1 1

(2 × 3) (6)

2.3

100 0100	D
100 1001	I
100 0111	G
100 1001	I
101 0100	T
101 0011	S

(6)
[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 3.1.1 True
3.1.2 False
3.1.3 True
3.1.4 False
3.1.5 True

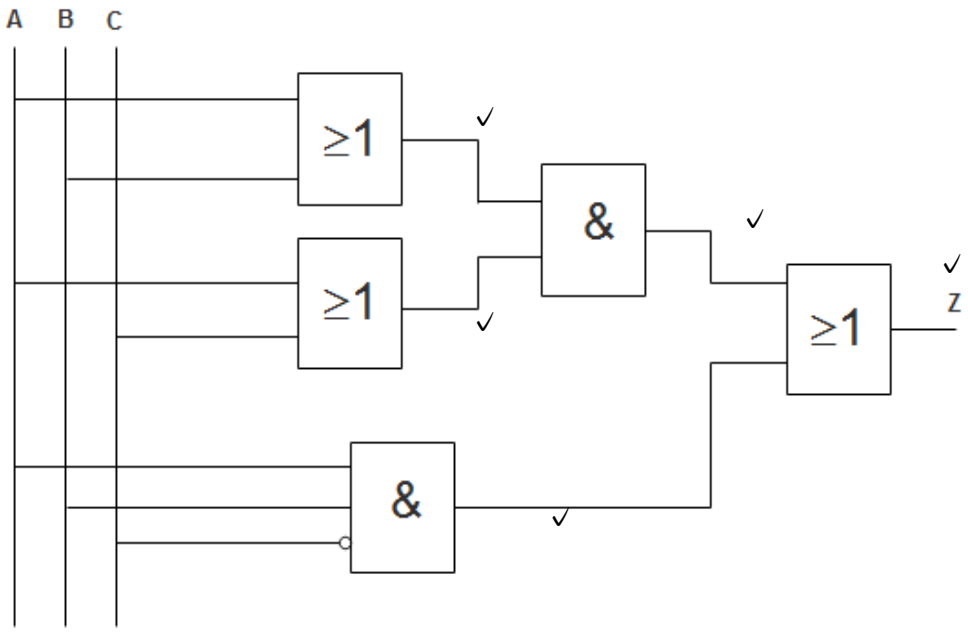
(5 × 1) (5)

3.2

A	B	C	a	b	c	d	Z
0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	1	1	1	0	0	0
1	0	0	1	0	0	0	0
1	0	1	1	0	1	1	0
1	1	0	1	0	0	0	0
1	1	1	1✓	0✓	0✓	0✓	0✓

(5)

3.3



(5)

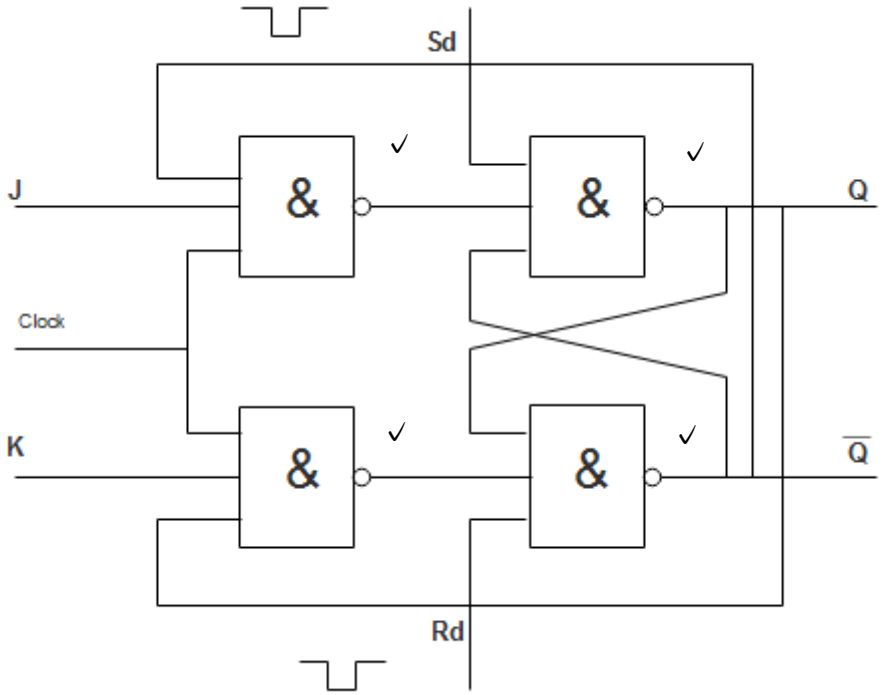
3.4 Emitter coupled logic (ECL)
Diode transistor logic (DTL)
Resistor transisor logic (RTL)
Integrated injector logic (IIL)
High threshold logic (HTL)
Alternate answers
Transistor transistor logic (TTL)
Schottky TTL
Direct coupled transistor logic (DCTL) (Any 5 × 1) (5)
[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 4.1.1 C
4.1.2 C
4.1.3 A
4.1.4 C
4.1.5 A
(5 × 1) (5)

4.2 4.2.1 Rewritable compact disc
4.2.2 Recordable compact disc
(2 × 2) (4)

4.3



If J = K = 0 and a clock pulse is applied to the flip flop, the output will remain unchanged.
If J = K = 1, then the output will toggle and
If J = 1 and K = 0, then the 1 will be carried over to the output by a clock pulse. (7)

4.4
- A combinational circuit is a circuit where the output in dependant only on the inputs at the same instant in time.
- A sequential circuit is a circuit in which the output does not only depend on the present inputs but also on the past inputs. (2 × 2) (4)

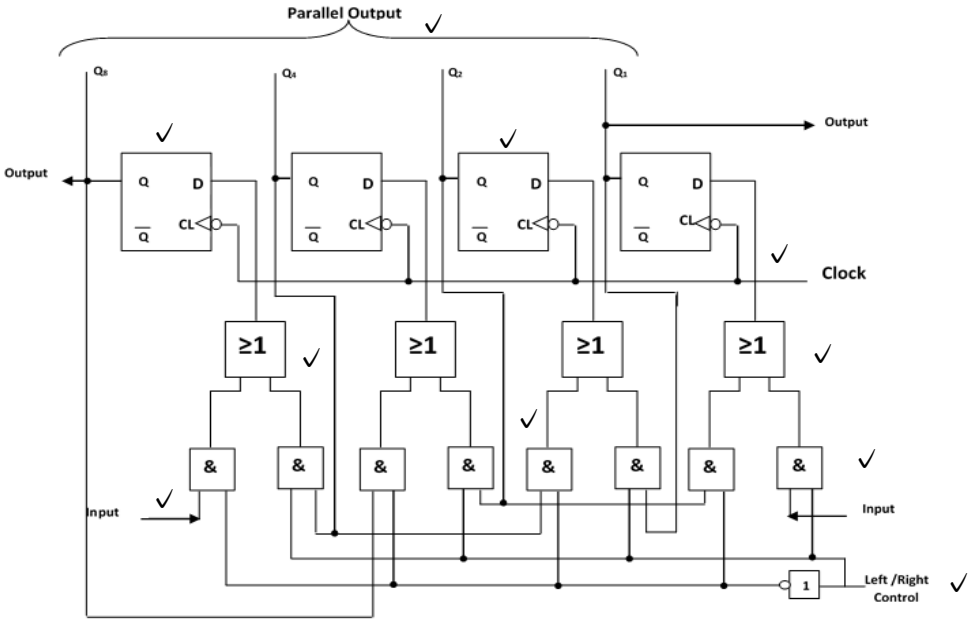
[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1
5.1.1 D
5.1.2 C
5.1.3 A
5.1.4 C
5.1.5 A

(5 × 1) (5)

5.2

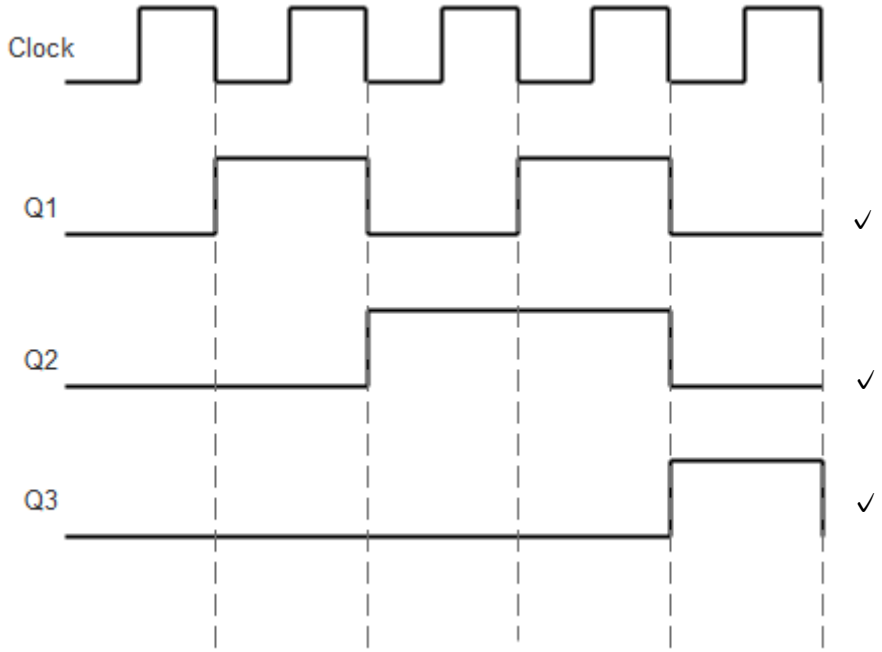


(10)

5.3

Clock Pulse	Q4	Q2	Q1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

✓ ✓



(5)
[20]

TOTAL: 100

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