higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T870**(E)**(A5)T
APRIL EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N3

(8080273)

5 April 2016 (X-Paper)
9:00–12:00

Calculators may be NOT used.

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. ALL the sketches and diagrams must be large, clear and neat.
5. Keep questions and subsections of questions together.
6. Show ALL the steps and calculations.
7. Write neatly and legibly.

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QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

1.1 If $X = 64_{16}$, $Y = 24_8$ and $Z = 15_{10,}$ calculate the following:

1.1.1 The value of X in the octal number system (2)

1.1.2 The product of Y and Z in the binary number system (4)

1.1.3 X divided by Y in the binary number system (3)

1.1.4 Use 2's complement to subtract 144_8 from X. (4)

1.2 Complete the following TRUTH TABLE by filling in the missing binary digits. Write only the answer next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

Inputs			**Outputs**	
A	B	C_{in}	Sum	C_{out}
0	0	0	1.2.1	0
0	0	1	1	0
0	1	0	1.2.2	0
0	1	1	0	1.2.3
1	0	0	1	0
1	0	1	0	1
1	1	0	1.2.4	1
1	1	1	1	1.2.5

TABLE 1 (5)

1.3 Briefly describe a half-adder. (2)

[20]

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 Give an example of each of the following codes:

2.1.1 Self-complementing weighted code

2.1.2 Non-weighted code

(2 × 1) (2)

2.2 What does *ASCII* stand for? (2)

2.3 Give ONE function of an encoder. (2)

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2.4 Convert the following numbers to the indicated code:

2.4.1 $111101001101_{2421BCD}$ code to decimal

2.4.2 103_{10} to XS3 (excess 3) code

(2 × 3) (6)

2.5 The following word is received at the end of a transmission data line:

1 0 1 1 1 0 1 1
1 0 0 0 1 0 1 1
1 1 1 0 0 1 0 0
1 0 1 0 1 1 0 0
1 0 0 0 1 1 1 1
1 1 1 1 1 1 1 1

By using even parities, determine whether any faults occurred during transmission and if so, rectify the fault(s). (8)

[20]

QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES

3.1 One way to think of logic gate types is to consider what input states guarantee a certain output state.

For example, an AND gate could be described as the function whereby any LOW input guarantees a LOW output.

Identify what type of gate is represented by each of the following statements:

3.1.1 Any LOW input guarantees a HIGH output.

3.1.2 Any difference in the input guarantees a LOW output.

3.1.3 Any HIGH input guarantees a HIGH output.

(3 × 2) (6)

3.2 Show, by means of a circuit diagram, how diodes can be used to construct an OR gate. (5)

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3.3 Study FIGURE 1 below and answer the questions.

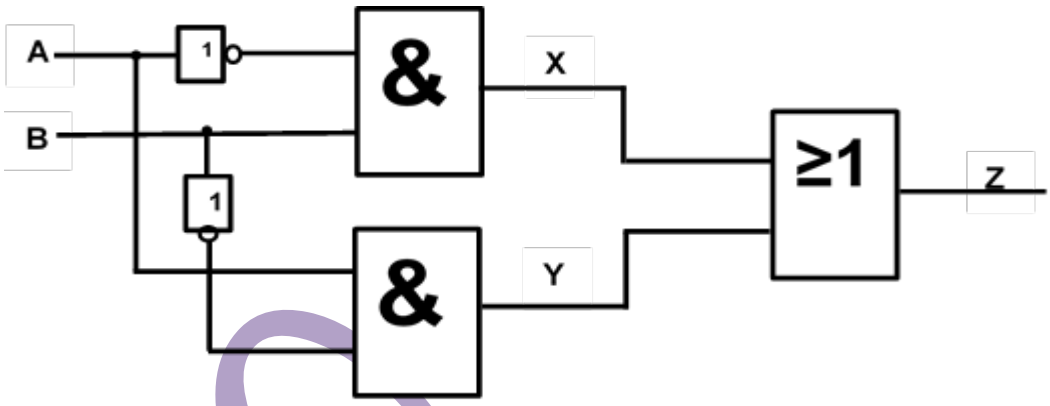

FIGURE 1

3.3.1 Copy the TRUTH TABLE below in your ANSWER BOOK and use FIGURE 1 above to complete it. (4)

INPUTS		OUTPUTS		
A	**B**	**X**	**Y**	**Z**
1	1			
0	1			
1	0			
0	0			

3.3.2 What type of logic gate is represented by output Z in FIGURE 1? (2)

3.3.3 Draw the IEC symbol for the logic gate identified in QUESTION 3.3.2. (2)

3.4 What is the minimum number of inputs that an AND gate can have? (1)

[20]

QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Choose an answer from COLUMN B that matches a description in COLUMN A. Write only the letter (A–G) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

COLUMN A		COLUMN B	
4.1.1	Time required to change the voltage level from 90% to 10%	A	edge triggering
4.1.2	Minimum time the data signal should be held steady before the clock event, so that the data is reliably sampled by the clock	B	rising time
4.1.3	A flip-flop triggered by either the positive edge or negative edge of the clock pulse	C	holding time
4.1.4	Time required to change the voltage level from 10% to 90%	D	falling time
4.1.5	Minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop	E	level triggering
		F	delay time
		G	setup time

(5 × 1) (5)

4.2 Briefly explain the difference between a combinational- and a sequential circuit. (4)

4.3 Study FIGURE 2 below and then answer the questions.

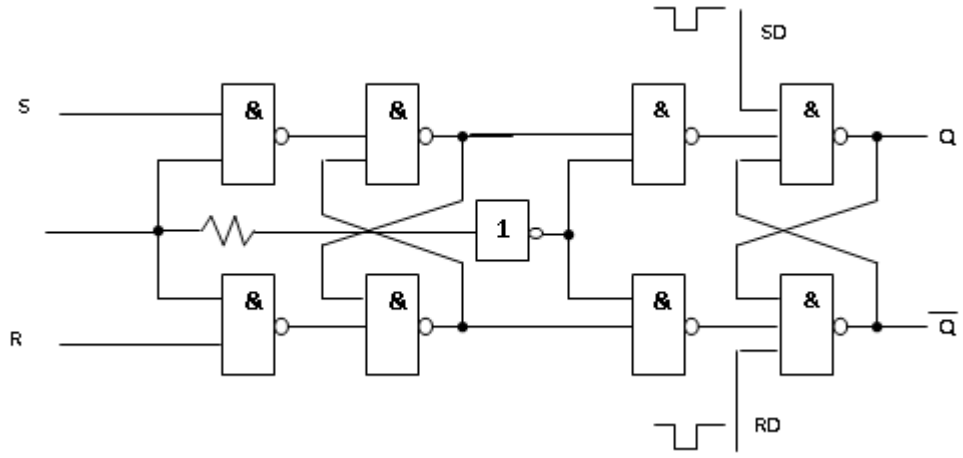

FIGURE 2

4.3.1 When a 1 is applied to both the set (S) and reset (R) inputs of the flip-flop in FIGURE 2 above the outputs are termed to be invalid.

Why are the outputs invalid? (2)

4.3.2 Draw the IEC symbol for the flip-flop in FIGURE 2. (2)

4.4 Draw a labelled single-cell structure for a dynamic read-write memory (DRAM). (5)

4.5 An SRAM cell has three different operating states of which one is standby.

Name the remaining TWO modes of operation. (2)
[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Explain the working principle of a 4-bit SISO (series-in-series-out) shift register. (12)

5.2 Draw a neat, labelled sketch of 4-bit ring counter making use of a JK flip-flop which is negatively edged. (8)
[20]

TOTAL: 100

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