higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N3

5 APRIL 2016

This marking guideline consists of 8 pages.

Copyright reserved

QUESTION 1

1.1 1.1.1 $X = 64_{16} = 01100100_2$✓
$= 001\ 100\ 100$
$= 144_8$✓
$\therefore Y = 144_8$ (2)

1.1.2 $Y = 24_8$ and $Z = 15_{10}$

		8	4	2	1
15 =		**1**	**1**	**1**	**1**

$\therefore 15_{10} = 1111_2$ ✓

	2	4
24_8 =	**010**	**100**

$\therefore 24_8 = 10100_2$ ✓

				1	0	1	0	0		
				x	1	1	1	1		
				1	0	1	0	0		
			1	0	1	0	0			✓
		1	0	1	0	0				
	1	0	1	0	0					
1	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**		✓

(4)

1.1.3 $X = 64_{16} = 1100100_2$

$Y = 24_8 = 10100$

							1	0	1	✓	
1	0	1	0	0	1	1	0	0	1	0	0
					1	0	1	0	0	↓	↓ ✓
					0	0	1	0	1	0	↓
						0	1	0	1	0	0 ✓
						0	0	0	0	0	0

(3)

1.1.4 $X = 1100100_2$

	1	4	4
144_8 =	**001**	**100**	**100**

$\therefore 144_8 = 1100100_2$ ✓

2's complement of 1100100 is equal to 0011011 + 1✓ = 0011100✓

	1	carry	↰							
	0	*	1	1	0	0	1	0	0	
	1	*	0	0	1	1	1	0	0	
1	0	*	0	0	0	0	0	0	0	✓
↳	ignore									

(4)

1.2 1.2.1 0
1.2.2 1
1.2.3 1
1.2.4 0
1.2.5 1

(5 × 1) (5)

1.3 A half-adder is an arithmetic element which has two inputs and two outputs (sum and carry out),✓ and it can add two bits at a time.✓ (2)
[20]

QUESTION 2

2.1 2.1.1 2421; 4221; 8421; 5211; 3321 or 4321 (Any 1) (1)

2.1.2 Gray or XS3 code (1)

2.2 American Standard Code for Information Interchange (2)

2.3 An encoder is used to convert decimal code to binary or BCD code. (2)

2.4 2.4.1

1 1 1 1	0 1 0 0	1 1 0 1
↓	↓	↓
2 4 2 1	2 4 2 1	2 4 2 1
↓	↓	↓
9✓	4✓	5✓

2.4.2

1	0	3
↓	↓	↓
1	0	3
+3	+3	+3
4	3	6
↓	↓	↓
0100✓	0011✓	0110✓

(2 × 3) (6)

2.5

1	0	1	1	**1**	0	1	1	e	
1	0	0	0	**1**	0	1	1	e	
1	1	1	0	**0**	1	0	0	e	✓
1	0	1	0	**1**	1	0	0	e	
1	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**u**	✓
1	1	1	1	**1**	1	1	1	e	
e	e	e	e	**u**	e	e	e		✓
	✓			✓		✓			

The fault is in column 5, row 5, the 1 (one) is changed to a 0 (zero)

1	0	1	1	**1**	0	1	1
1	0	0	0	**1**	0	1	1
1	1	1	0	**0**	1	0	0
1	0	1	0	**1**	1	0	0
1	**0**	**0**	**0**	**0✓✓**	**1**	**1**	**1**
1	1	1	1	**1**	1	1	1

(8)
[20]

QUESTION 3

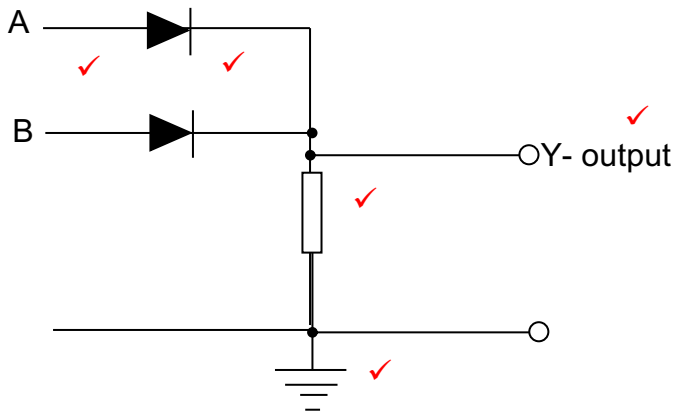
3.1 3.1.1 NAND gate

3.1.2 XNOR gate

3.1.3 OR gate

(3 × 2) (6)

3.2



- 1 mark for direction of diode
- 1 mark for right connection of diodes
- 1 mark for resistor
- 1 mark for output
- 1 mark for earthing

(5)

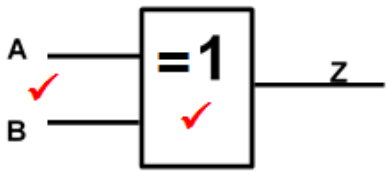
3.3 3.3.1

INPUTS		OUTPUTS		
A	**B**	**X✓**	**Y✓**	**Z✓✓**
1	1	0	0	**0**
0	1	1	0	**1**
1	0	0	1	**1**
0	0	0	0	**0**

(4)

3.3.2 XOR gate (1 x 2) (2)

3.3.3



(2)

3.4 One (1) (1)

[20]

QUESTION 4

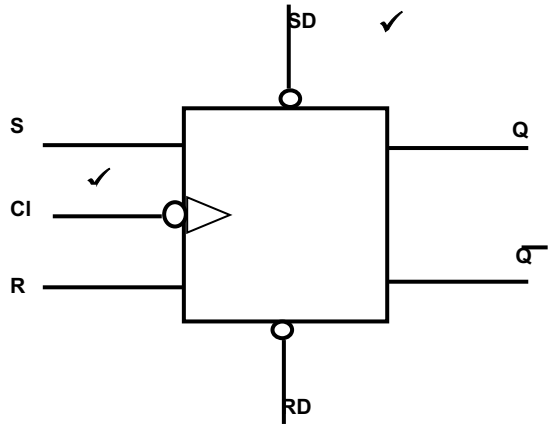
4.1
4.1.1 D
4.1.2 G
4.1.3 A
4.1.4 B
4.1.5 C

(5 × 1) (5)

4.2 A combinational circuit can be defined as a circuit of which the output is dependent only on the inputs✓ at the same instant of time✓ whereas a sequential circuit can be defined as a circuit of which the output depends not only on the present inputs✓ but also on the past history of inputs. (4)

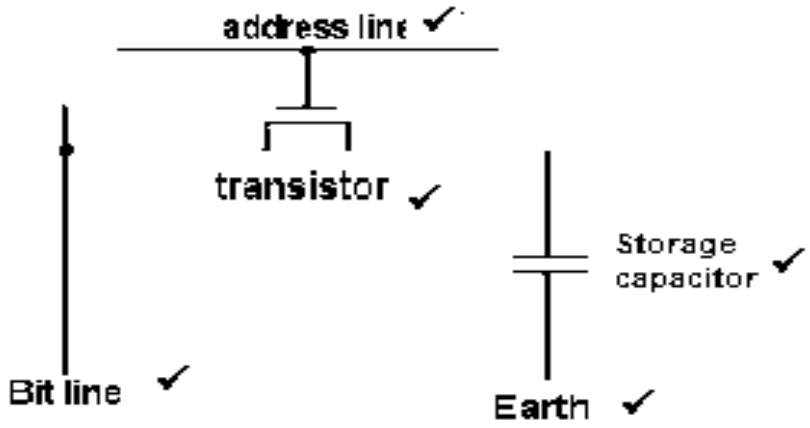
4.3 4.3.1 The outputs are invalid because the outputs of both **Q** and **Q'** go to 0.✓ This condition violates the fact that the outputs are complements of each other.✓ (2)

4.3.2



(2)

4.4



(5)

4.5
- Reading mode
- Writing mode

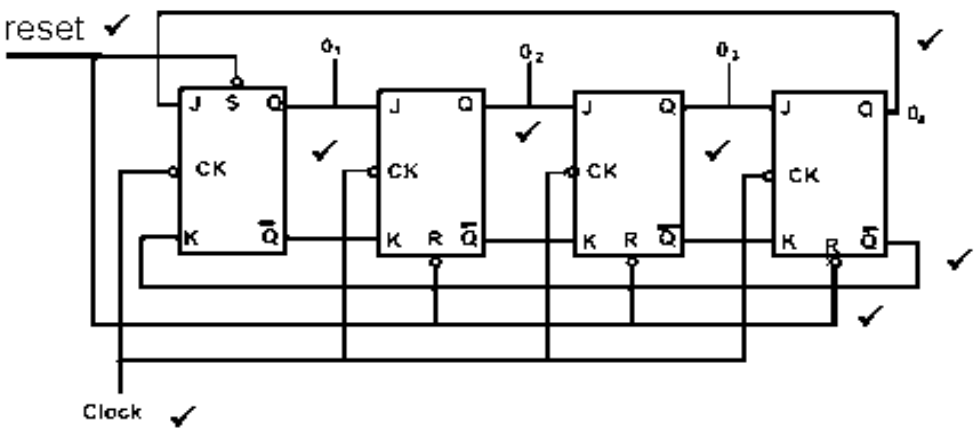
(2)
[20]

QUESTION 5

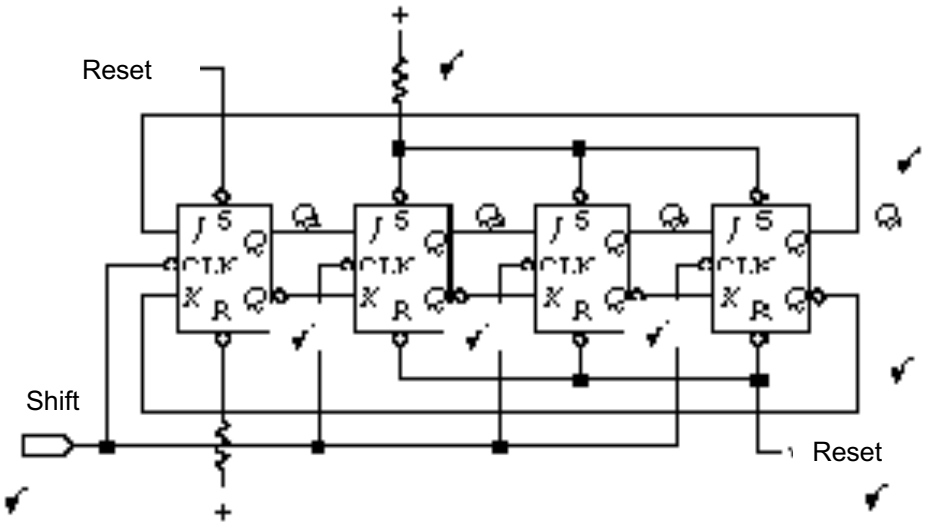
5.1

1. Bit 0 is entered into the data input line. *D1* = 0, first clock pulse is applied, *FF1* is reset and stores 0.✓
2. Next bit 1 is entered. Q1 = 0, since *Q1* is connected to *D2, D2* becomes 0.✓
3. Second clock pulse is applied, the 1 on the input line is shifted into *FF1* because *FF1* sets. The 0 which was stored in *FF1* is shifted into *FF2.*✓
4. Next bit 0 is entered and third clock pulse applied. 0 is entered into *FF1,* 1 stored in *FF1* is shifted to *FF2* and 0 stored in *FF2* is shifted to *FF3.*✓
5. Last bit 1 is entered and 4th clock pulse applied.✓ 1 is entered into *FF1,* 0 stored in *FF1* is shifted to *FF2,*✓ 1 stored in *FF2* is shifted to *FF3* and 0 stored in *FF3* is shifted to *FF4.* This completes the serial entry of 4-bit data into the register. Now the LSB 0 is on the output Q4.✓
6. Clock pulse 5 is applied. LSB 0 is shifted out. The next bit 1 appears on Q4 output.✓
7. Clock pulse 6 is applied. The 1 on Q4 is shifted out and 0 appears on Q4 output.✓
8. Clock pulse 7 is applied. 0 on Q4 is shifted out. Now 1 appears on Q4 output. ✓
9. Clock pulse 8 is applied. 1 on Q4 is shifted out. ✓
10. When the bits are being shifted out (on CLK pulse 5 to 8) more data bits can be entered. ✓ (12)

5.2



OR



(8)
[20]

TOTAL: 100

Copyright reserved