higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N3

7 APRIL 2015

This marking guideline consists of 7 pages.

Copyright reserved

SECTION A

QUESTION 1

1.1	1.1.1	B ✓	(1)
	1.1.2	D✓	(1)
	1.1.3	B✓	(1)
	1.1.4	B✓	(1)
	1.1.5	D✓	(1)
	1.1.6	C✓	(1)
	1.1.7	C✓✓	(2)
	1.1.8	C✓✓	(2)
1.2	1.2.1	False✓	(1)
	1.2.2	True✓	(1)
	1.2.3	False✓✓	(2)
	1.2.4	True✓	(1)
	1.2.5	False✓	(1)
	1.2.6	False✓	(1)
	1.2.7	True✓	(1)
	1.2.8	True✓	(1)
	1.2.9	False✓	(1)
1.3	1.3.1	C	
	1.3.2	E	
	1.3.3	B	
	1.3.4	D	
	1.3.5	A	

(5 × 1) (5)
[25]

TOTAL SECTION A: 25

Copyright reserved

SECTION B

QUESTION 2

2.1 $10010111_2 - 78_{16}$

128	64	32	16	8	4	2	1
1	0	0	1	0	1	1	1

$\therefore 10010111 = 128 + 16 + 4 + 2 + 1 = 151_{10}$ ✓

$(7 \times 16^1) + (8 \times 16^0) = 112 + 8 = 120_{10}$ ✓

Ten's complement of 120 is 1 000 – 120 = 880 ✓

$$\begin{array}{cccccc} & 0 & * & 1 & 5 & 1 \\ & 1 & * & 8 & 8 & 0 \\ \hline 1 & 0 & * & 0 & 3 & 1 \end{array}$$ ✓

↳ ignore carry (4)

2.2 $37_8 \times 1000_2$

3	7
011	111

$\therefore 37_8 = 11111_2$ ✓

$$\begin{array}{ccccccccc} & & & 1 & 1 & 1 & 1 & 1 \\ & & & & 1 & 0 & 0 & 0 \\ \hline & & & 0 & 0 & 0 & 0 & 0 \\ & & 0 & 0 & 0 & 0 & 0 & \\ & 0 & 0 & 0 & 0 & 0 & & \checkmark \\ 1 & 1 & 1 & 1 & 1 & & & \\ \hline 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \checkmark \end{array}$$

128	64	32	16	8	4	2	1
1	1	1	1	1	0	0	0

$\therefore 11111000 = 128 + 64 + 32 + 16 + 8 = 248_{10}$ ✓ (4)

Copyright reserved

2.3 $64_{16} \div 1010_2$

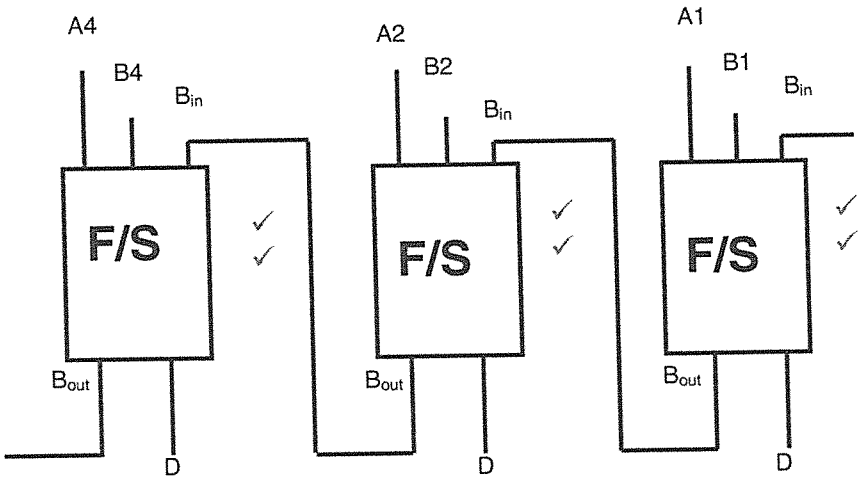
6	4
0110	0100

$\therefore 64_{16} = 1100100_2$ ✓

```
                    1   0   1   0   ✓
1   0   1   0 | 1   1   0   0   1   0   0
              | 1   0   1   0
              |-----------------
              | 0   0   1   0   1
              |     0   0   0   0       ✓
              |-----------------
                    1   0   1   0
                    1   0   1   0
                    -----------------
                    0   0   0   0   0
                    -----------------
                            0
```

$\therefore 1010_2 = A_{16}$ ✓ (4)

2.4 3-bit parallel subtractor.



(6)

2.5 21 to XS3

```
  2     1                  2     1
 +3    +3                  ↓     ↓
 ----------------  OR   0010  0001
  5     4                + 11  + 11
 ----------------      ----------------
 ↓✓    ↓✓               0101✓ 0100✓
0101  0100
```

(2)

2.6 100 0001 → A✓
101 0011 → S✓
100 0011 → C✓
100 1001 → I ✓
100 1001 → I ✓ (5)

Copyright reserved

2.7

BCD input				Input
2✓	4✓	2✓	1✓	Decimal ✓
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
1	0	1	1	5
1	1	0	0	6
1	1	0	1	7
1	1	1	0	8
1	1	1	1	9

(5)
[30]

QUESTION 3

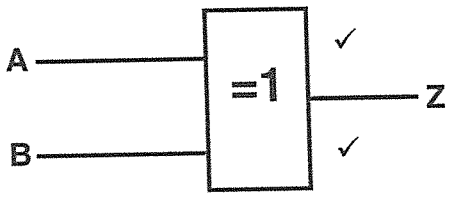
3.1 3.1.1

Inputs		Outputs		
		✓✓	✓✓	✓✓
A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

(6)

3.1.2 Exclusive OR (XOR) gate ✓✓ (2)

3.1.3



(2)

3.2 Advantage: bipolar IC has higher speed/it is faster than MOS IC.✓✓
Disadvantage: bipolar IC uses more power than MOS IC.✓✓ (4)

3.3 12✓ (1)
[15]

Copyright reserved

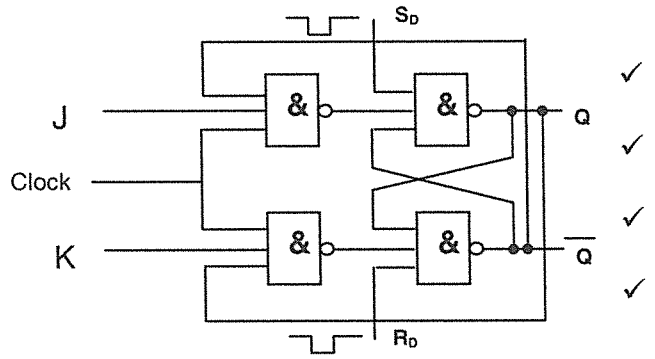
QUESTION 4

4.1 4.1.1 The small triangle at the clock input depicts positive-edge triggering✓✓

4.1.2 The circle symbol (together with the small triangle) represents negative-edge triggering.✓✓

(2 × 2) (4)

4.2



✓ ✓ ✓ ✓

If J = K = 0 and clock pulse is applied to the flip-flop, the output will remain unchanged✓
If J = K = 1, then the output will toggle (switch over to the opposite position with every clock pulse); and✓
If J = 1, K = 0, then the 1 will be carried over to the output by a clock pulse ✓ (7)

4.3 4.3.1 CD-RW stands for rewritable compact disc.✓✓

4.3.2 CD-R stands for recordable compact disc.✓✓

(2 × 2) (4)
[15]

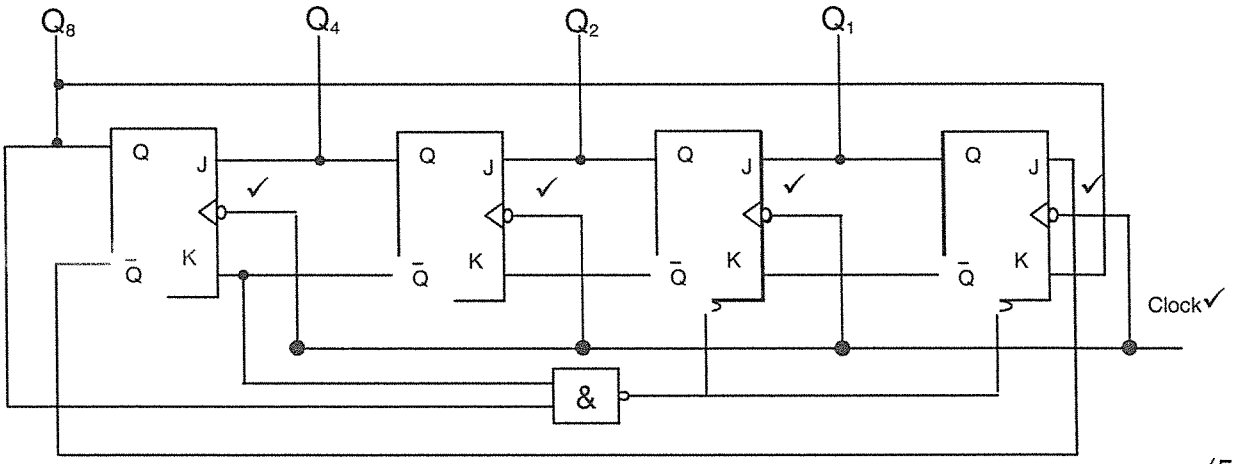
Copyright reserved

QUESTION 5

5.1 5.1.1 0000✓✓ (2)

5.1.2 1110 and 1001✓✓ (2)

5.2



(5)

5.3 5.3.1 1010, 1011, 1110 and 1111 (4)

5.3.2 0011 (Or ANY four-bit binary number. Why? Because the initial content of the down-counter is UNKNOWN.)✓✓ (2)

[15]

TOTAL SECTION B: 75
GRAND TOTAL: 100

Copyright reserved