higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T850(E)(N27)T
**NOVEMBER EXAMINATION**

**NATIONAL CERTIFICATE**

# LOGIC SYSTEMS N2

(8080262)

**27 November 2014 (Y-Paper)**
**13:00–16:00**

**Calculators may NOT be used.**

**This question paper consists of 6 pages.**

ENGINEERING

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# DEPARTMENT OF HIGHER EDUCATION AND TRAINING
# REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

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**INSTRUCTIONS AND INFORMATION**

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

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## QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 Which statement below best describes the function of a decoder?

A A decoder will convert a decimal number into the proper binary equivalent.

B A decoder will convert a binary number into a specific output representing a particular character or digit.

C Decoders are used to prevent improper operation of digital systems.

D Decoders are special ICs that are used to make it possible for one brand of computer to talk to another.

1.1.2 A NOT gate added to a NOR gate will give the following:

A NOR gate
B NAND gate
C OR gate
D AND gate

1.1.3 12 is a decimal number for a binary:

A 0011
B 1100
C 0110
D 1010

1.1.4 A four-bit shift register will store decimal numbers up to the following:

A Fifteen
B Eight
C Ten
D Four

1.1.5 An output of a full-subtractor is in the form of the following:

A Borrow out and difference
B Borrow out
C Sum
D Difference

(5 x 1) (5)

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1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.10) in the ANSWER BOOK.

1.2.2 A parallel counter is also known as a synchronous counter.

1.2.3 Bidirectional shift registers can shift data either right or left.

1.2.5 A full-adder adds three bits, a half-adder adds one and a half bits.

1.2.7 ROM stands for read-write-memory.

1.2.10 The most significant digit is the rightmost, largest-weight digit in a number.

(5 x 1) (5)
**[10]**

**SECTION B**

**QUESTION 2**

2.1 Give FOUR binary-addition rules. (4)

2.2 Convert each of the following numbers to their BINARY equivalents and then perform the calculations in the binary-number system:

2.2.2 $50_{10} - 101101_{10}$ [convert the answer to the decimal number system] (4)

2.2.3 $15_{10} \times 1100_2$ (4)

2.2.4 $1100100_2 \div 1010_2$ [convert the answer to the decimal number system] (5)

2.3 Draw a fully labelled logic-circuit diagram of a full-subtractor using half-subtractors and an OR gate. (7)

2.4 Convert 269 to the codes as indicated below:

2.4.1 2421 BCD code (3)

2.4.3 XS3 binary equivalent (3)

2.5 Draw a neat, labelled logic circuit for a 8421 BCD encoder (6)

2.6 What is the difference between an encoder and a decoder? (4)
**[40]**

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## QUESTION 3

3.1 Redraw and complete TABLE 1 below according to the gates indicated on the table.

| Inputs | | Outputs | | |
|---|---|---|---|---|
| A | B | AND | NOR | XOR |
| 0 | 0 | | | |
| 1 | 1 | | | |
| 1 | 0 | | | |
| 0 | 1 | | | |

**TABLE 1** (6)

3.2 Draw the IEC symbol for a TWO-input NAND gate. (2)

3.3 Draw the switch circuit for a NOT gate. (3)

3.4 What type of gate will be obtained when the output of a NOR gate is connected to a NOT gate? (2)

3.5 Study FIGURE 1 below and answer the questions.

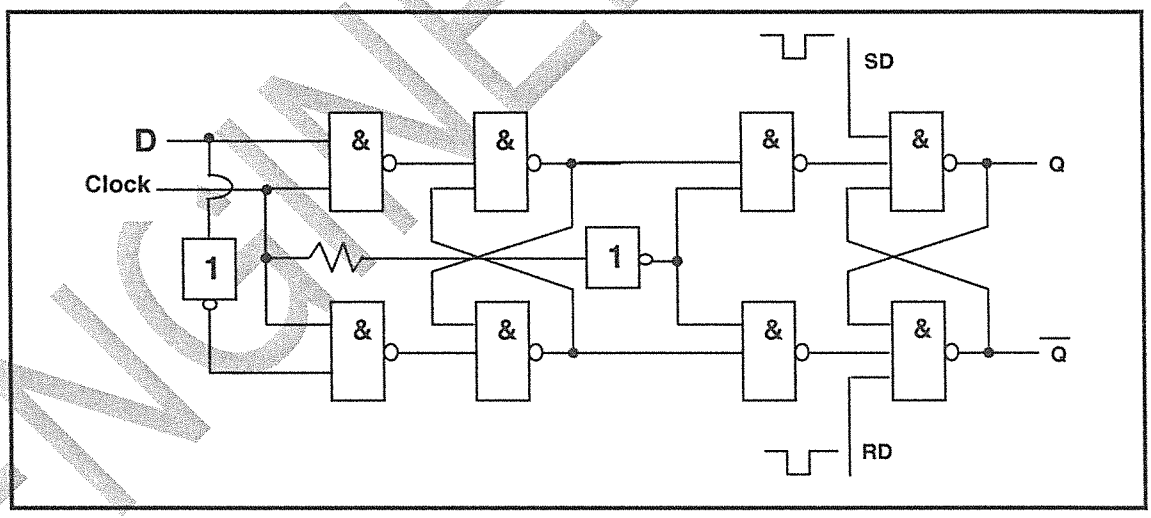



**FIGURE 1**

3.5.1 Identify the type of flip-flop represented by FIGURE 1 above. (2)

3.5.2 What type of flip-flop will be obtained if the NOT gate between the set and reset input is removed? (2)

3.5.3 Draw the truth table for the flip-flop in QUESTION 3.5.2 above. (3)

3.5.4 If output Q in FIGURE 1 above is logic 0 (zero), then what will the value of output $\overline{Q}$ be? (1)

3.6 Give FOUR types of secondary memory. (4)

**[25]**

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## QUESTION 4

4.1 What are the similarities between a parallel-in series-out shift register and parallel-in parallel-out shift register? (2)

4.2 Draw a fully labelled circuit diagram of a shift register using D-type flip-flops with the following features: parallel input, parallel output and output control. (10)

4.3 Re-draw and complete the following truth table for a FOUR-bit binary down-counter. (5)

| Clock pulses | Q8 | Q4 | Q 2 | Q1 |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | | |
| 2 | | | | |
| 3 | | | | |
| 4 | | | | |
| 5 | | | | |
| 6 | | | | |
| 7 | | | | |
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |
| 15 | | | | |

4.4 Draw a neat, labelled circuit diagram of a FOUR-bit decimal counter using JK-type flip-flops. (8)
**[25]**

**TOTAL: 100**

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