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higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T930(E)(M22)T
APRIL EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

22 March 2013 (X-Paper)
09:00–12:00

Calculators may NOT be used.

This question paper consists of 5 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

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QUESTION 1

1.1 Convert each of the following decimal numbers to their BINARY equivalents and then complete the calculations in the BINARY number system:

1.1.1 21 + 35 + 12 (5)

1.1.2 44 ÷ 11 (5)

1.2 Calculate the following numbers in BINARY number systems and convert the final answer to DECIMAL number system:

1.2.1 110010 – 11011 (3)

1.2.2 1100 x 111 (4)

1.3 Draw a fully labelled logic circuit diagram of a half-adder using NAND gates only. Also draw a truth table. (8)
[25]

QUESTION 2

2.1 Convert the following numbers to the code as indicated:

2.1.1 851 decimal to its 2421 BCD code (3)

2.1.2 100100110110 8421 BCD code to its decimal equivalent (3)

2.1.3 100100110110 XS3 to it decimal equivalent (3)

2.2 Draw a neat, labelled logic circuit for a 2421 BCD encoder. (10)

2.3 What is the difference between an *encoder* and a *decoder*? (4)

2.4 Name TWO types of logic gates which are used to construct a decoder. (2)
[25]

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QUESTION 3

3.1 Study the logic gates below and answer the questions. Write only the answer next to the letter (a–c) in the ANSWER BOOK.

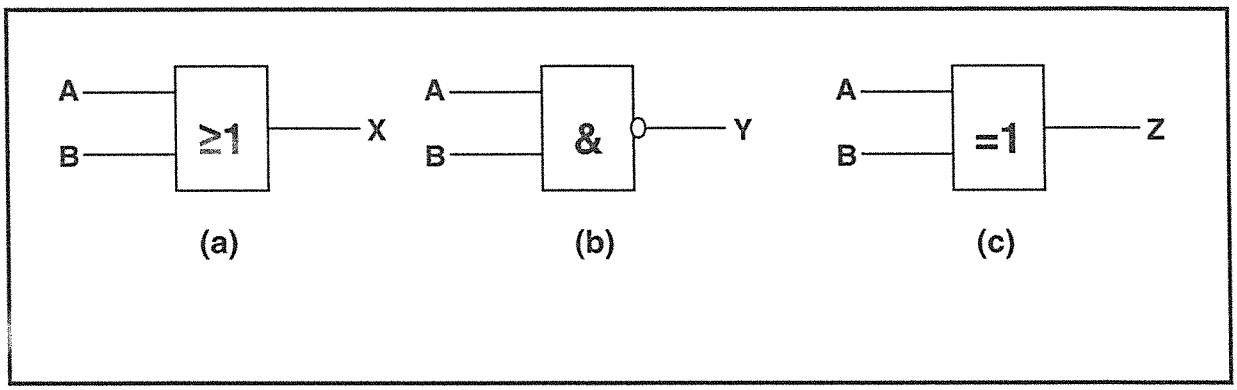


FIGURE 1

3.1.1 Identify the names of the gates represented by FIGURE 1 above. (3)

3.1.2 Complete TABLE 1 below by making use of the gates in FIGURE 1 above. (6)

INPUT		OUTPUT		
A	B	X	Y	Z
0	0			
0	1			
1	0			
1	1			

TABLE 1

3.1.3 Draw the switch circuit for the gate represented by FIGURE 1(a). (3)

3.2 List FOUR different types of flip-flop. (4)

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3.3 Study FIGURE 2 below and answer the questions.

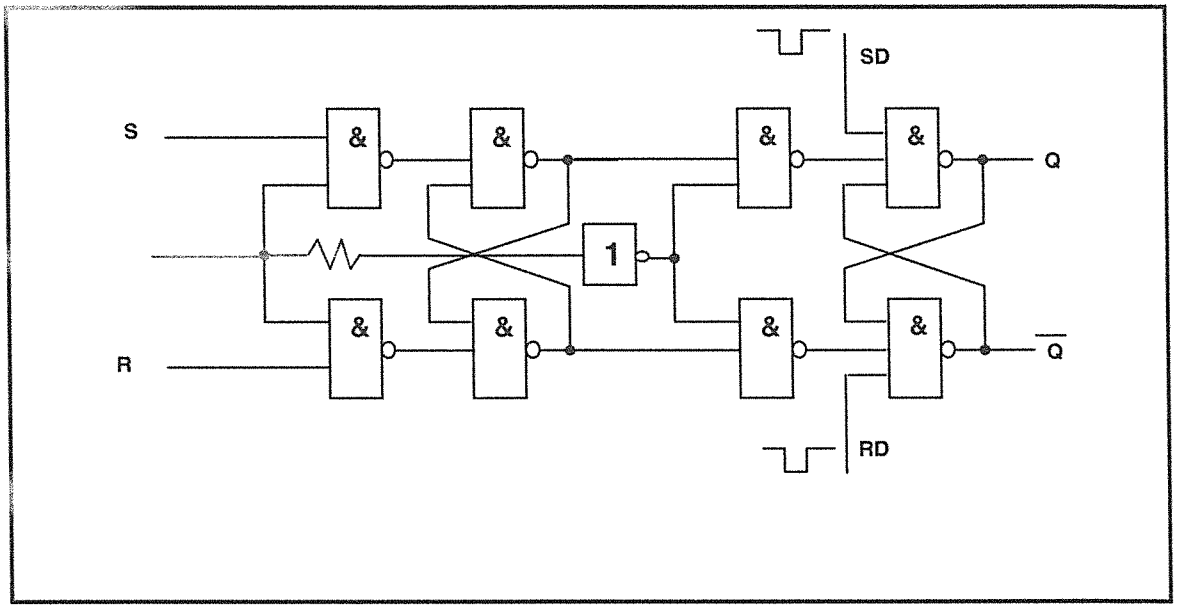


FIGURE 2

3.3.1 What type of flip-flop is represented in FIGURE 2? (2)

3.3.2 Draw the truth table for the flip-flop in QUESTION 3.3.1. (2)

3.3.3 Draw the IEC symbol for the flip-flop in QUESTION 3.3.1. (3)

3.4 Name TWO types of main (primary) memory. (2)
[25]

QUESTION 4

4.1 Name FIVE groups of shift registers. (5)

4.2 Draw a fully labelled circuit diagram of a shift register using D-type flip-flops with the following features: series input, parallel output and output control. (10)

4.3 Why are asynchronous counters also called series counters? (2)

4.4 Draw a neat, labelled circuit diagram of an asynchronous down counter using J-K-type flip-flops. (8)
[25]

TOTAL: 100

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