higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N2

22 MARCH 2013

This marking guideline consists of 8 pages.

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QUESTION 1

1.1 1.1.1 21 + 35 + 12

	32	16	8	4	2	1	
21 =		1	0	1	0	1	✓
35 =	1	0	0	0	1	1	✓
12 =			1	1	0	0	✓

```
        1 0 1 0 1
      1 0 0 0 1 1
  +       1 1 0 0
  ---------------
  1 0 0 0 1 0 0   ✓✓
  ---------------
```

(5)

1.1.2 44 ÷ 11

	32	16	8	4	2	1	
44 =	1	0	1	1	0	0	✓
11 =			1	0	1	1	

```
                  1 0 0 ✓
1 0 1 1 | 1 0 1 1 0 0
          1 0 1 1
          0 0 0 0 0   ✓
            0 0 0 0
            0 0 0 0 0
              0 0 0 0 ✓
              0 0 0 0
```

(5)

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1.2 1.2.1 110010 – 11011

	1	1	0	0	1	0	
-		1	1	0	1	1	
		1	**0**	**1**	**1**	**1**	✓

16	8	4	2	1
1	0	1	1	1

$\therefore 10111_2 = 16 + 4 + 2 + 1 = 23_{10}$ ✓✓ (3)

1.2.2 110 x 111

			1	1	0	
		x	1	1	1	
			1	1	0	
		1	1	0		✓
	1	1	0			
	1	**0**	**1**	**0**	**1**	**0** ✓

32	16	8	4	2	1
1	0	1	0	1	0

$\therefore 101010_2 = 32 + 8 + 2 = 42_{10}$ ✓✓ (4)

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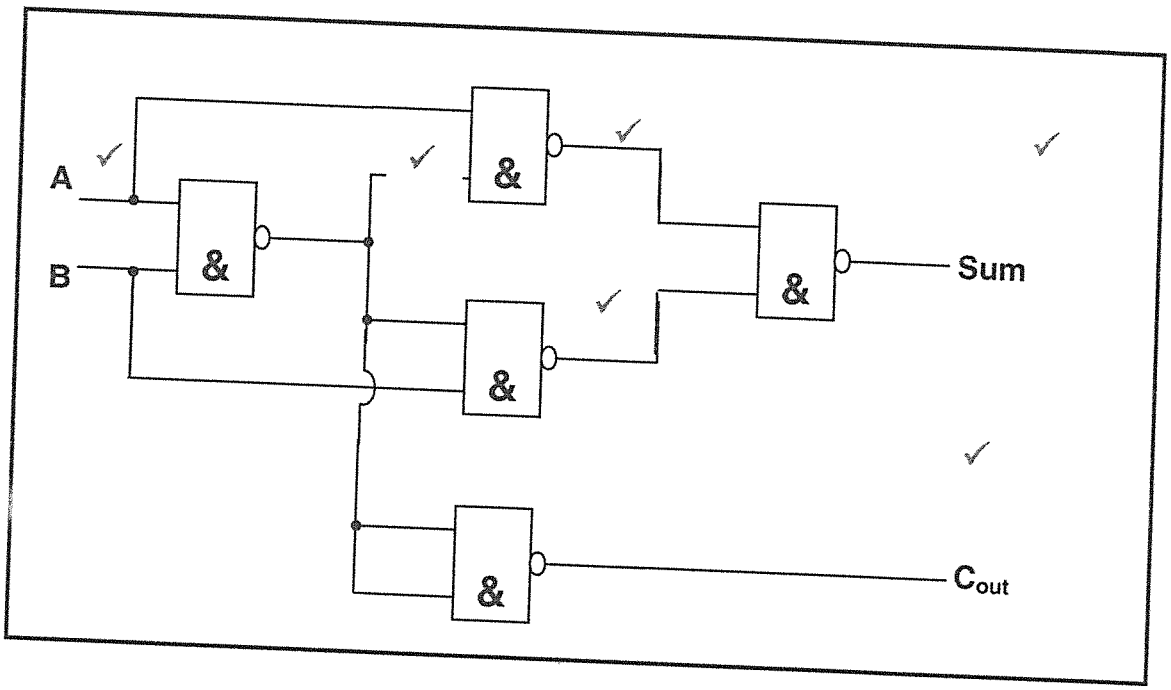
1.3



CIRCUIT DIAGRAM

Truth table

A	B	Sum ✓	C_{out} ✓
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(8)
[25]

QUESTION 2

2.1 2.1.1 851 decimal to its 2421 BCD code

2421	2421	2421
8	5	1
↓✓	↓✓	↓✓
1110	**1011**	**0001**

(3)

2.1.2 100100110110 8421 BCD code to its decimal equivalent.

8421	8421	8421
1001	0011	0110
↓✓	↓✓	↓✓
9	**3**	**6**

(3)

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2.1.3 100100110110 XS3 to it decimal equivalent.

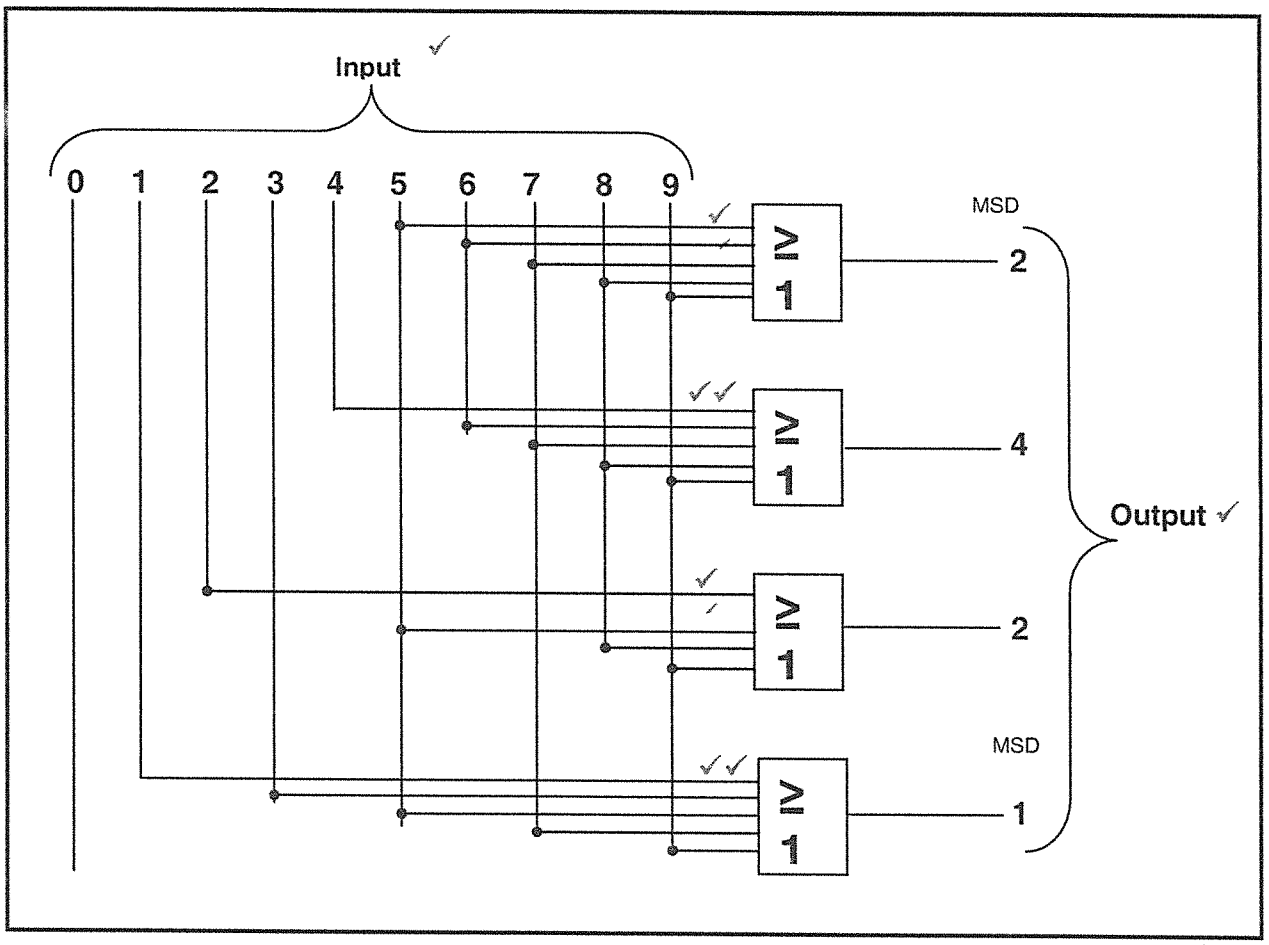
1001	0011	0110
- 11	- 11	- 11
0110	0000	0011
↓	↓	↓
6✓	0✓	3✓

OR

1001	0011	0110
↓	↓	↓
9	3	6
- 3	-3	-3
6✓	0✓	3✓

(3)

2.2



(10)

LOGIC CIRCUIT

2.3 A decoder changes a binary or BCD code to a decimal code, ✓✓while an encoder changes a decimal code to a binary or BCD code. ✓✓ (4)

2.4 AND gate✓ and NOT gate✓ (2)

[25]

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QUESTION 3

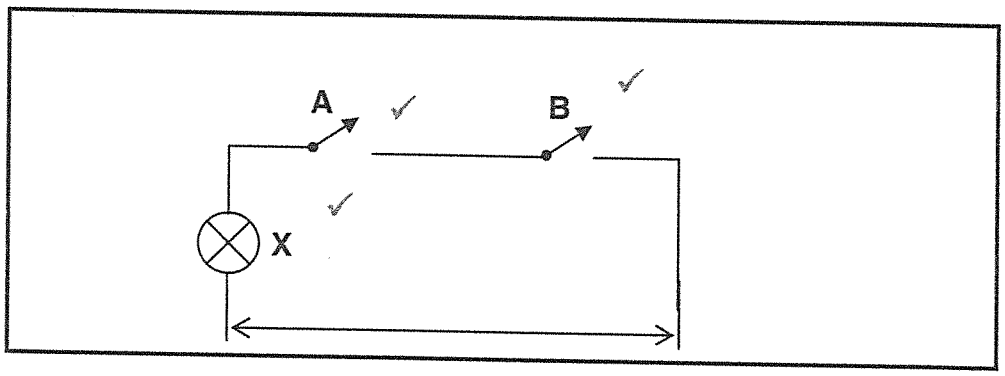
3.1 3.1.1 (a) OR gate✓
(b) NAND gate✓
(c) XOR gate ✓ (3)

3.1.2

Input		Output		
A	B	X ✓✓	Y ✓✓	Z ✓✓
0	0	0	1	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	0

TABLE 1 (6)

3.1.3



SWITCH CIRCUIT (3)

3.2 SR flip-flop ✓
JK flip-flop ✓
T flip-flop ✓
D flip-flop ✓ (4)

3.3 3.3.1 SR master/slave (2)

3.3.2

S	R	Q	
0	0	Q_n	$\overline{Q}$ ✓
0	1	0	$\overline{Q_n}$ ✓
1	0	1	0
1	1	Invalid	

(2)

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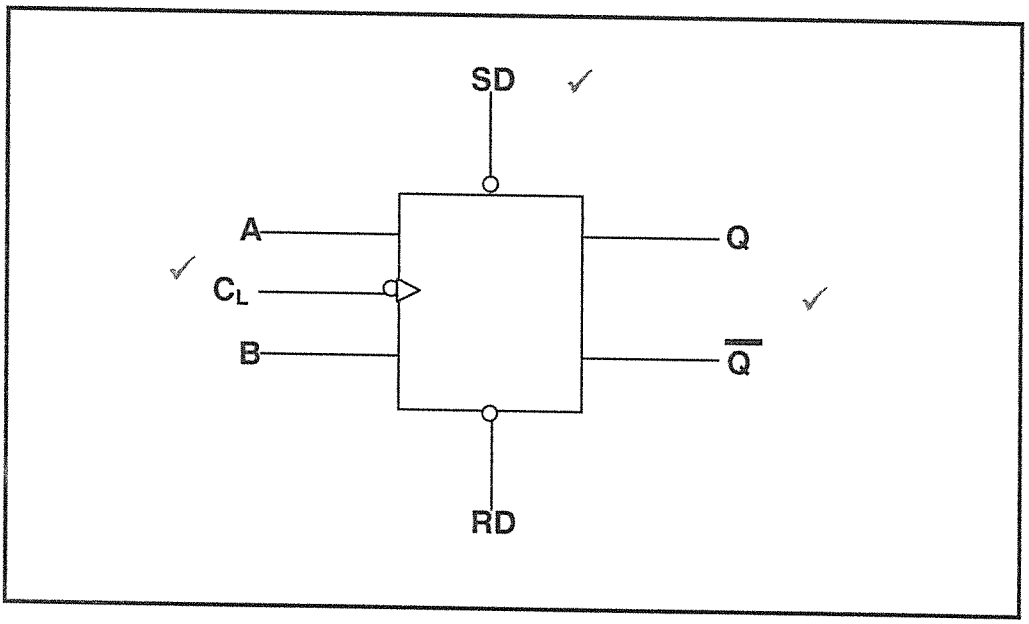
3.3.3



(3)

IEC SYMBOL

3.4 Magnetic core ✓
Semiconductor ✓

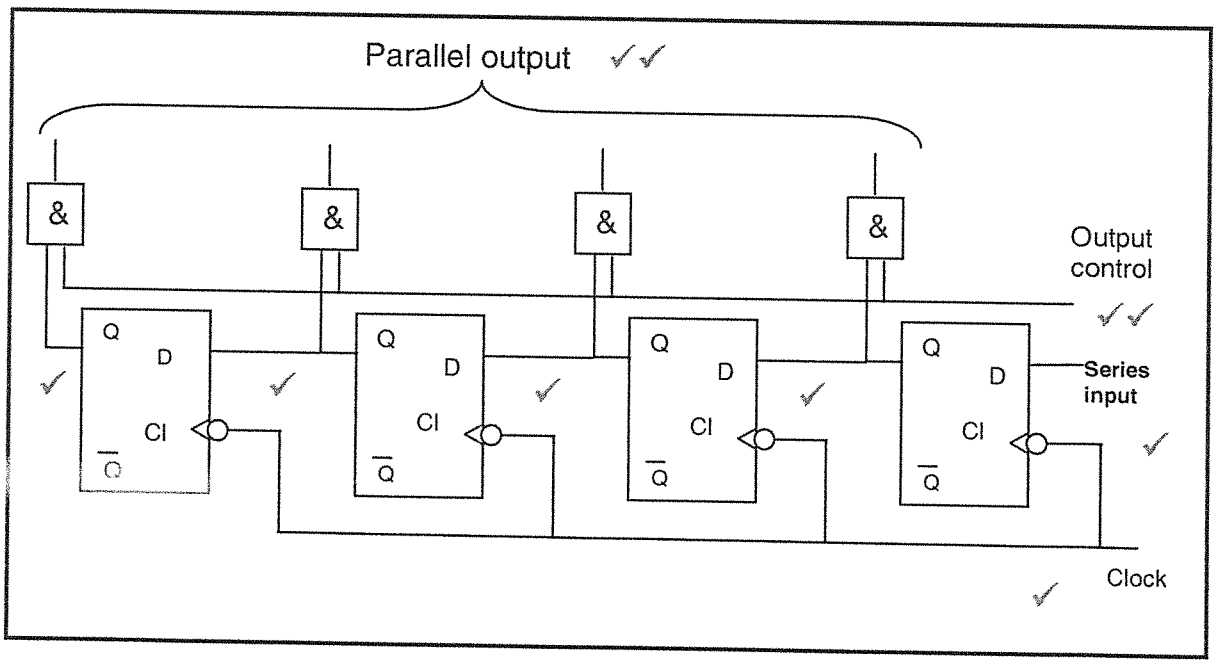
(2)
[25]

QUESTION 4

4.1 Parallel-in parallel-out register ✓
Parallel-in series-out register ✓
Series-in series-out register ✓
Series-in parallel-out register ✓
Ring counter ✓

(5)

4.2



(10)

SHIFT REGISTER

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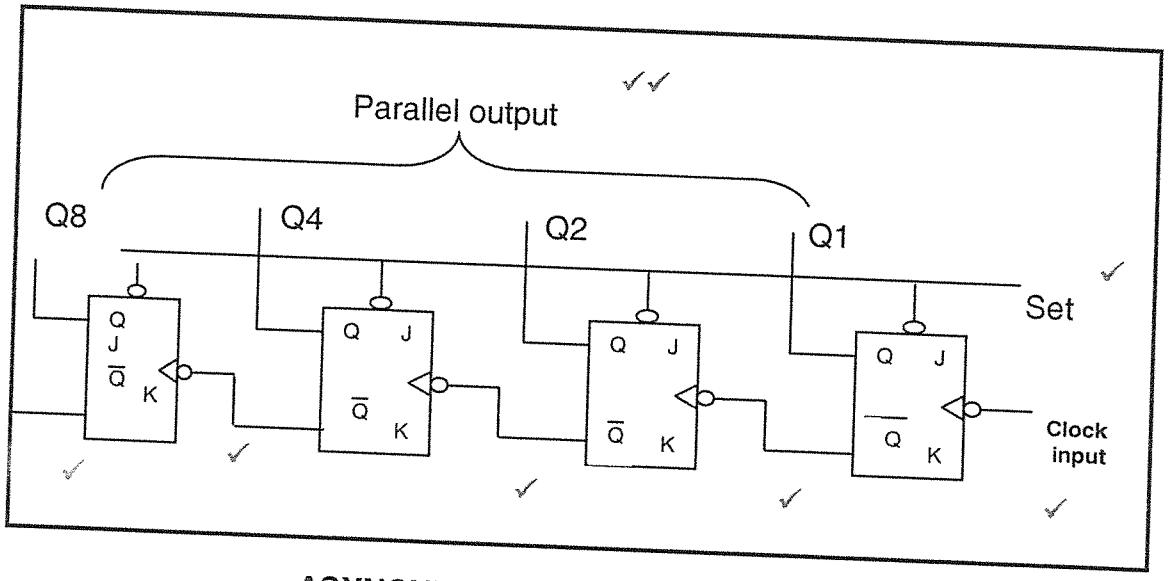
4.3 Because an output of one flip-flop is a clock of the next one ✓✓ (2)

4.4



(8)
[25]

ASYNCHRONOUS DOWN COUNTER

TOTAL: 100

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