higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

19 November 2021

This marking guideline consists of 6 pages.

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QUESTION 1

1.1 1.1.1 Addition
1.1.2 Subtraction
1.1.3 Addition

(3 × 1) (3)

1.2 0 + 0 = 0✓
0 + 1 = 1✓
1 + 0 = 1✓
1 + 1 = 0 with a carry of 1✓ (4)

1.3

A	B	C	D	E	Q	
0	0	0	1	0	1	✓
0	0	1	1	0	1	✓
0	1	0	0	0	0	✓
0	1	1	0	1	1	✓
1	0	0	0	0	0	✓
1	0	1	0	0	0	✓
1	1	0	0	0	0	✓
1	1	1	0	1	1	✓

(8)

1.4 1.4.1

Code	8	4	2	1
14 =	**1**	**1**	**1**	**0**

Therefore, 14 = 1110_2 ✓

Code	8	4	2	1
13 =	**1**	**1**	**0**	**1**

Therefore, 14 = 1101_2 ✓

```
    1 1 1 0
x   1 1 0 1
    0 0 0 0
  1 1 1 0 0
1 1 1 0 0 0   ✓
+ 1 1 1 0 0 0 0
1 1 0 0 0 1 0 0₂  ✓✓
```

(5)

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1.4.2

Code	32	16	8	4	2	1
56 =	**1**	**1**	**1**	**0**	**0**	**0**

Therefore, 14 = 1110_2 ✓

Code	4	2	1
4 =	**1**	**0**	**0**

Therefore, 14 = 1110_2 ✓

```
          1 1 1 0₂  ✓
  1 0 0 | 1 1 1 0 0 0
        - 1 0 0
            1 1 0    ✓
          - 1 0 0
              1 0 0
            - 1 0 0
                  00 ✓
                  00
```

(5)
[25]

QUESTION 2

2.1 2.1.1 A
2.1.2 A
2.1.3 A
2.1.4 B
2.1.5 B

(5 × 1) (5)

2.2 2.2.1 Encoder: An encoder converts decimal characters to binary code✓ for central processor to perform arithmetic operations in binary. ✓

2.2.2 Decoder: A decoder converts binary code ✓to decimal characters to be displayed. ✓

(2 × 2) (4)

2.3 2.3.1 $101001001_{8421BCD}$

0001 0100 1001✓
8421 8421 8421✓
1 4 9

$101001001_{8421BCD}$ = 149✓ (3)

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2.3.2 $101001011000_{XS3CODE}$

1010	0101	1000	
-0011	-0011	-0011	✓
0111	0010	0101	
8421	8421	8421	✓
7	2	5	

$101001011000_{XS3CODE}$ = 725✓ (3)

2.4

Decimal	BCD(5421)				
	A	B	C	D	✓
0	0	0	0	0	
1	0	0	0	1	✓
2	0	0	1	0	✓ ✓
3	0	0	1	1	
4	0	1	0	0	✓
5	1	0	0	0	✓
6	1	0	0	1	✓
7	1	0	1	0	✓
8	1	0	1	1	
9	1	1	0	0	✓

(10)
[25]

QUESTION 3

3.1
- Bit density
- Speed
- Power consumption
- Storage cost
- Convenience

(5)

3.2 The JK flip-flop has the advantage that, no non-permissible combination can ✓be placed on the input. ✓ (2)

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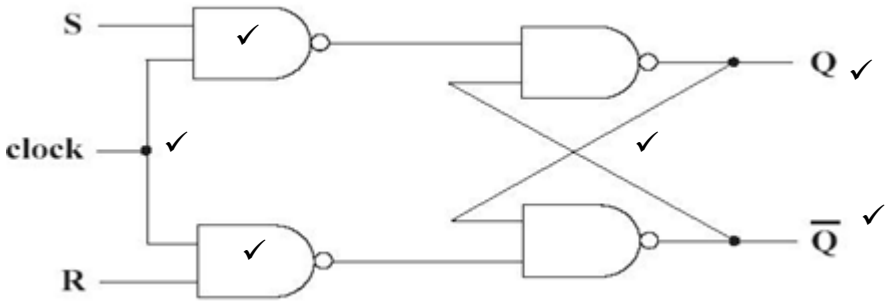
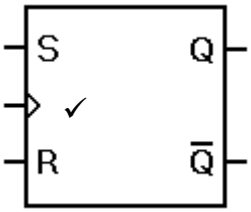
3.3 3.3.1



(6)

3.3.2



(2)

3.3.3

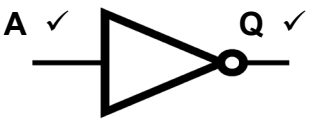
(4)

S✓	R✓	Q ✓	$\overline{Q}$ ✓
0	0	Q_n	$\overline{Q}_n$
0	1	0	1
1	0	1	0
1	1		

3.4 3.4.1 The inverter is the logic gate that has only one input✓ and it outputs the opposite logic state of its input✓ (2)

3.4.2

(2)



3.4.3

(2)

A	Q
0	1
1	0

[25]

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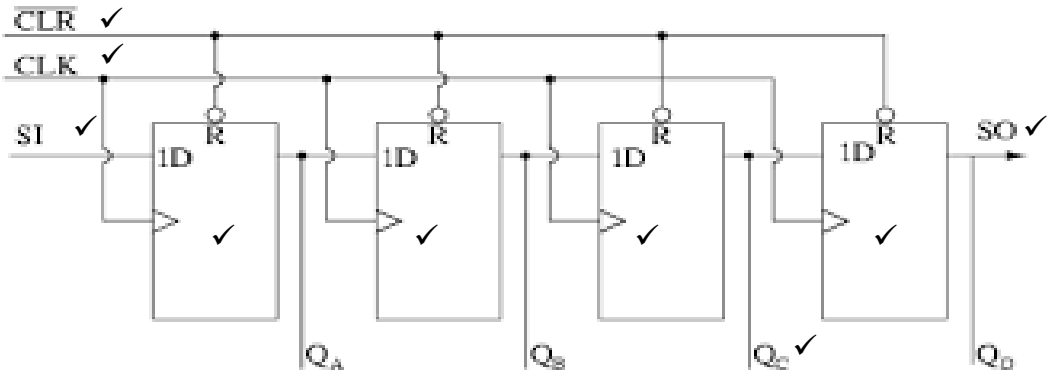
QUESTION 4

4.1 Left shift registers ✓
Right shift registers✓
Bidirectional shift registers **or** left and right shift registers✓
Circular shift registers ✓ (4)

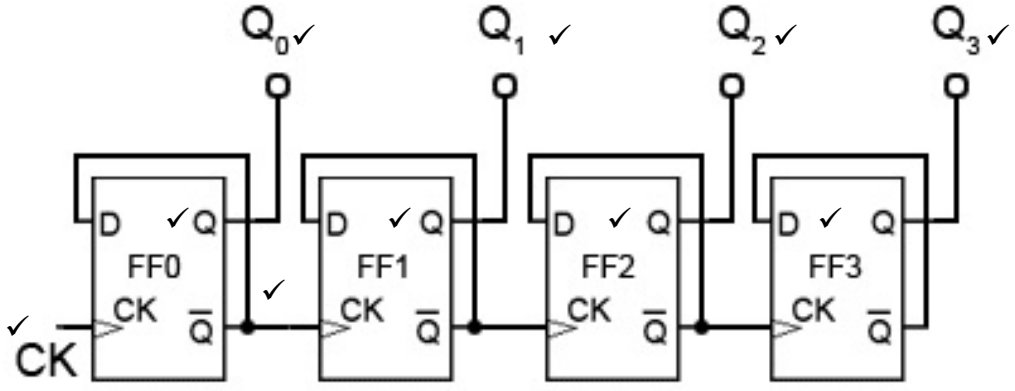
4.2
- Serial-in, Parallel-out
- Serial-in, Serial-out
- Parallel-in, Serial-out
- Parallel-in, Parallel-out (Any 2 × 1) (2)

4.3



Serial-in/ Parallel out shift register details (9)

4.4



(10)
[25]

TOTAL: 100

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