higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T920**(E)**(A1)T

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

1 August 2019 (X-Paper)
09:00–12:00

NO calculators may be used.

This question paper consists of 5 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Start each question on a NEW page.
5. ALL sketches and diagrams must be large, clear and neat.
6. Keep questions and subsections of questions together.
7. Answer questions in blue or black ink and make ALL drawings with a pencil.
8. Show ALL calculations.
9. Write neatly and legibly.

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QUESTION 1

1.1 How many different combinations can be indicated with four bits? (1)

1.2 Give FOUR binary subtraction rules. (4)

1.3 The table below shows arithmetic calculations in binary number systems.

Complete the table by writing only the answer next to the question number (1.3.1–1.3.8) in the ANSWER BOOK.

Decimal		Binary		Operation	Results in binary
23_{10}	**1.3.1**	10111_2	1001_2	**1.3.2**	1110_2
17_{10}	45_{10}	10001_2	**1.3.3**	Addition	**1.3.4**
1.3.5	10_{10}	**1.3.6**	1010_2	Division	1010_2
22_{10}	6_{10}	**1.3.7**	110_2	**1.3.8**	10000100_2

(8 × 1) (8)

1.4 Design a logic circuit diagram for a full adder by using the following logic gates:

- TWO AND gates
- TWO XOR gates
- ONE OR gate (7)

1.5 Draw the truth table for the logic circuit designed in QUESTION 1.4. (5)

[25]

QUESTION 2

2.1 The table below shows 4-bit weighted codes.

Copy and complete the table in the ANSWER BOOK.

2.1.1

Decimal	7421	$8\overline{4}\overline{2}\overline{1}$
0	0000	0000
1	0001	**2.1.1.1**
2	**2.1.1.2**	0110
3	0011	**2.1.1.3**
4	**2.1.1.4**	0100
5	0101	**2.1.1.5**
6	**2.1.1.6**	1010
7	1000	**2.1.1.7**
8	**2.1.1.8**	1000
9	1010	**2.1.1.9**

(9 × 1) (9)

2.1.2 Which of the codes in QUESTION 2.1.1 is self-complementing? (1)

2.2 Name THREE gates that will produce an output of logic 1 only if one of the two inputs (i.e. A or B) is at logic 1. (3)

2.3 Draw a neat, labelled logic circuit for an 8421 BCD encoder. (10)

2.4 Complete the following paragraph by writing the missing word or words next to the question number (2.4.1–2.4.2) in the ANSWER BOOK.

When any (2.4.1) … number is pressed on the keyboard of a pocket calculator, the number is converted to a (2.4.2) … code which is acceptable to the central processor. (2 × 1) (2)

[25]

QUESTION 3

3.1 Give FIVE characteristics used to compare different memories. (5)

3.2 Briefly explain the difference between *set* and *preset* with reference to flip-flops. (4)

3.3 Make a neat, labelled sketch of a JK master-slave flip-flop. (8)

3.4 Copy and complete the following table relating to logic gates in the ANSWER BOOK:

LOGIC GATE	IEC SYMBOL	TRUTH TABLE
NAND	**3.4.1**	**3.4.2**
3.4.3		**3.4.4**

(4 × 2) (8)

[25]

QUESTION 4

4.1 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'True' or 'False' next to the question number (4.1.1–4.1.6) in the ANSWER BOOK.

4.1.1 A recirculating register is a register of which the serial output is connected to the serial input in a circulated manner.

4.1.2 A register is defined as the group of flip-flops suitable for storing decimal information.

4.1.3 D stands for data in the case of register not delay.

4.1.4 The register capable of shifting in one direction is the bidirectional shift register.

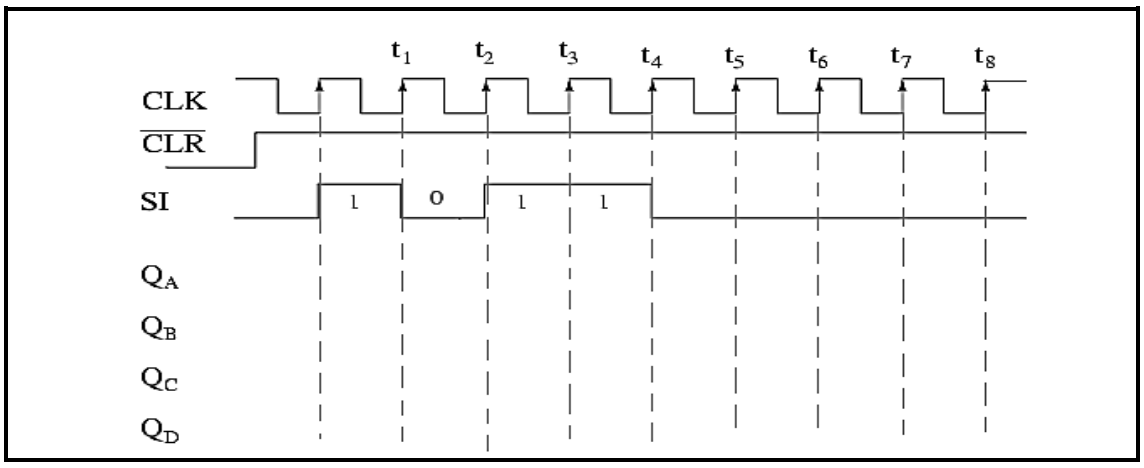
4.1.5 Two types of shifting of data are available, namely serial shifting and parallel shifting.

4.1.6 In a ripple counter the clock pulses are applied to one flip-flop only. Hence, as the number of flip-flops increases the delay increases.

(6 × 1) (6)

4.2 Below is a timing diagram for a series-in-series-out shift register.

Show how this data will be shifted to the output after FOUR clock pulses by redrawing and completing the diagram below in the ANSWER BOOK.



(9)

4.3 Why are asynchronous counters also called series counters? (2)

4.4 Draw a neat, labelled diagram of a 4-bit asynchronous binary counter. (8)

[25]

TOTAL: 100

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