higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T920(**E**)(J30)T

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

30 July 2018 (X-Paper)
09:00–12:00

Nonprogrammable calculators may be used.

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Keep questions and subsections of questions together.
5. ALL the sketches and diagrams must be large, clear and neat.
6. Show ALL the steps and calculations.
7. Write neatly and legibly

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SECTION A

QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.10) in the ANSWER BOOK.

1.1.1 Transformation of information into registers is called …

A loading.
B gated latch.
C latch.
D storing.

1.1.2 If excitation is not to be used, then the flip-flop used is … a/an

A JK flip-flop.
B RS flip-flop.
C T flip-flop.
D D flip-flop.

1.1.3 The decimal number 5 in 2421 coding is …

A 1011.
B 1001.
C 1010.
D 1100.

1.1.4 Ripple counters are also called …

A SSI counters.
B asynchronous counters.
C synchronous counters.
D VLSI counters.

1.1.5 The most preceded operator is …

A parenthesis.
B AND.
C OR.
D NOT.

1.1.6 The symbol for AND gate is …

A plus.
B minus.
C ampersand.
D dollar.

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1.1.7 All the inputs are synchronised with …

A a master clock.
B clock pulses.
C a counter.
D a latch.

1.1.8 A full adder consists of …

A 1 half adder.
B 2 half adders.
C 3 half adders.
D 4 half adders.

1.1.9 ROM is a …

A non-volatile memory.
B secondary memory.
C volatile memory.
D small memory.

1.1.10 The memory elements in clocked sequential circuits are called …

A latches.
B flip-flops.
C signals.
D gates.

(10 × 1) (10)

1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'True' or 'False' next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

1.2.1 The most significant digit is the rightmost, largest-weight digit in a number.

1.2.2 ROM stands for read-write-memory.

1.2.3 A full-adder adds three bits; a half-adder adds one and a half bits.

1.2.4 Bidirectional shift registers can shift data either right or left.

1.2.5 A parallel counter is also known as a synchronous counter.

(5 × 1) (5)
[15]

TOTAL SECTION A: 15

SECTION B

QUESTION 2

2.1 Explain what is meant by *self-complementing code* and give an example of a self-complementing code. (2)

2.2 Draw a neat, labelled logic circuit for an 8421 BCD decoder. (7)

2.3 Convert the following numbers to the indicated code:

2.3.1 60 to its binary XS3 equivalent (2)

2.3.2 111100111100 2421 BCD code to its decimal equivalent (3)

2.4 2.4.1 Draw an IEC symbol for a half-subtractor. (3)

2.4.2 Also draw the truth table. (3)

2.5 Calculate the following numbers in binary number systems and convert the final answer to the decimal number system:

2.5.1 $111111_2 - 11011_2$ (3)

2.5.2 $110_2 \times 1111_2$ (4)

2.6 Convert each of the following decimal numbers to their binary equivalents and then complete the calculations in the binary number system:

2.6.1 $25_{10} + 31_{10} + 10_{10}$ (4)

2.6.2 $120_{10} \div 15_{10}$ (4)

[35]

QUESTION 3

3.1 Study the logic circuit in FIGURE 1 below and answer the questions.

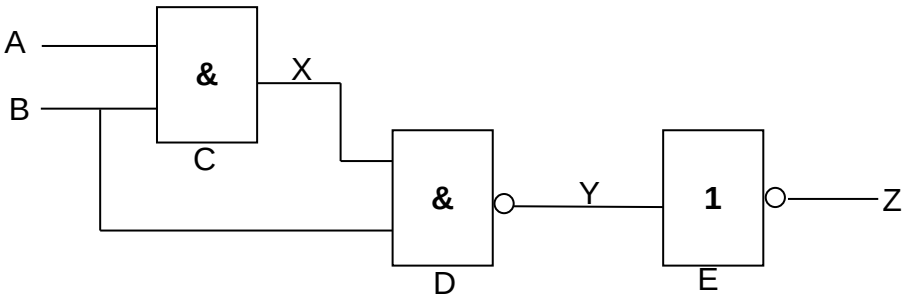


FIGURE 1

3.1.1 Identify the THREE digital gates used in FIGURE 1. (3)

3.1.2 Draw and complete the TABLE below in the ANSWER BOOK according to the gates indicated on the table.

INPUTS		OUTPUTS		
A	**B**	**X**	**Y**	**Z**
0	0			
1	1			
1	0			
0	1			

TABLE 1 (3)

3.2 The exclusive OR gate (XOR) is a digital logic gate that gives a true (1/HIGH) output when the number of true inputs is odd.

3.2.1 Give the IEC symbol for an XOR-gate with two inputs. (2)

3.2.2 Give the truth table an XOR-gate with two inputs. (3)

3.3 Draw the RS flip-flop using the NOR logic gates. (4)

3.4 Study the logic circuit in FIGURE 2 below and answer the questions.

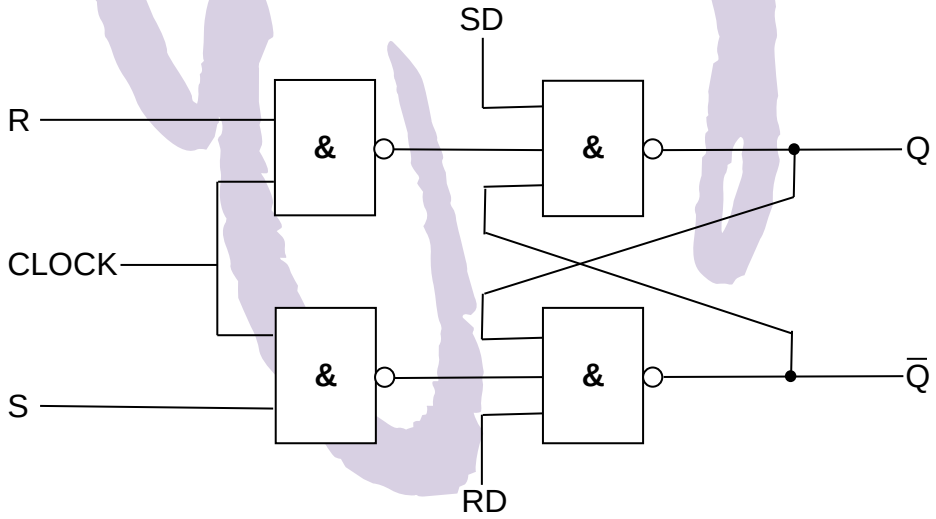


FIGURE 2

3.4.1 Identify and name the given flip-flop in FIGURE 2. (1)

3.4.2 Name the gates used in FIGURE 2. (1)

3.4.3 What will be the outputs of the flip-flop if S = 0 and R = 0? (1)

3.4.4 Draw the complete truth table for the flip-flop represented in FIGURE 2. (4)

3.4.5 Draw the IEC symbol of the truth table mentioned in QUESTION 3.4.4. (2)

3.5 What does CD-RW stand for? (1)

[25]

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QUESTION 4

4.1 Draw a neat, labelled circuit diagram of a 4-bit asynchronous up/down counter using JK-type flip-flops. (12)

4.2 Draw the truth table for a decade down-counter. (4)

4.3 List FIVE applications of a shift register. (5)

4.4 Briefly explain the difference between a *parallel-in parallel-out shift register* and a *series-in parallel-out shift register*. (4)
[25]

TOTAL SECTION B: 85
TOTAL: 100

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