higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

30 JULY 2018

This marking guideline consists of 7 pages.

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SECTION A

QUESTION 1

1.1	1.1.1	A
	1.1.2	D
	1.1.3	A
	1.1.4	B
	1.1.5	A
	1.1.6	C
	1.1.7	B
	1.1.8	D
	1.1.9	A
	1.1.10	B

(10 × 1) (10)

1.2	1.2.1	False
	1.2.2	False
	1.2.3	False
	1.2.4	True
	1.2.5	True

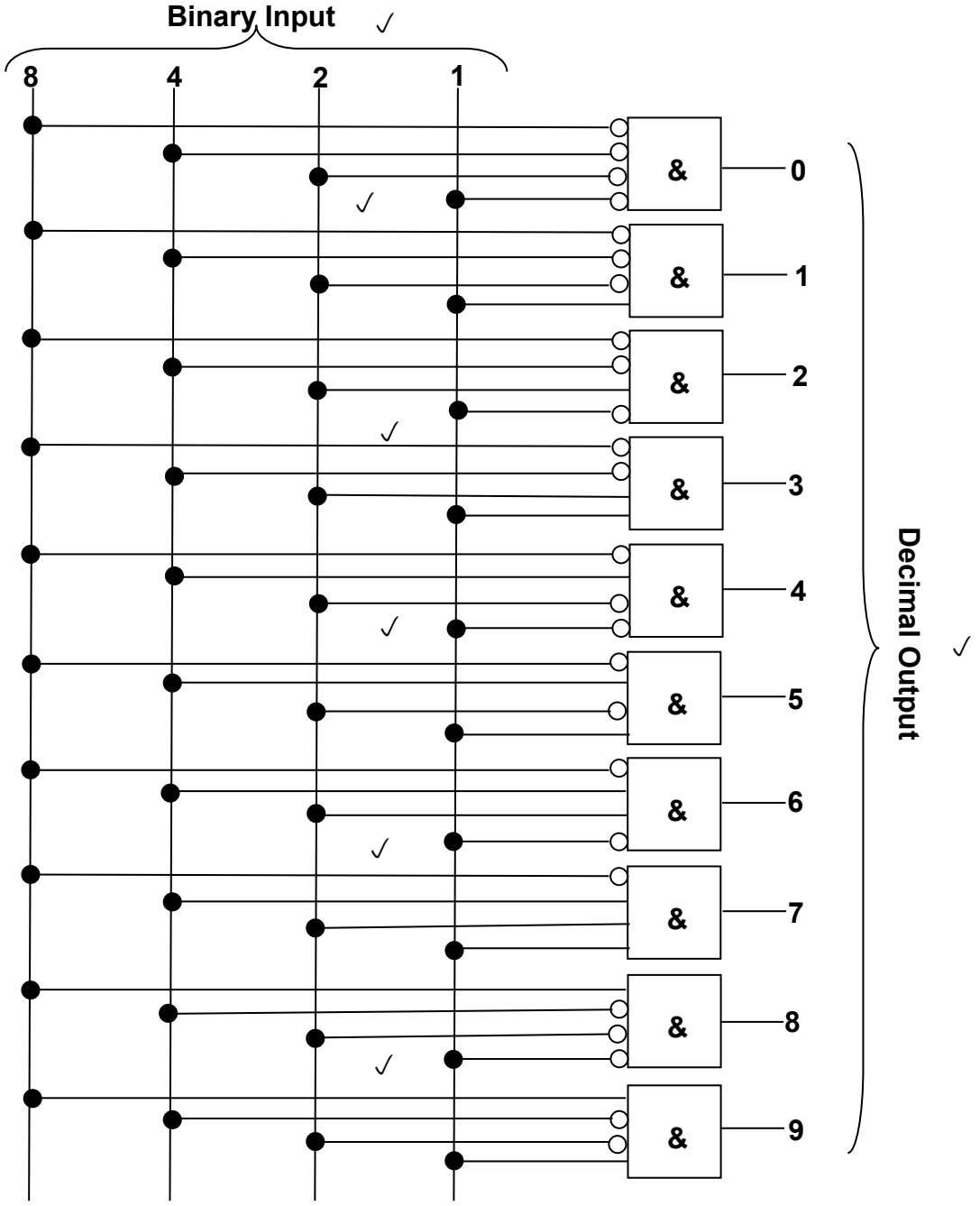
(5 × 1) (5)
[15]

SECTION B

QUESTION 2

2.1 A code is self-complementing if 1's complement of the code number of *x* gives the code number of 9 – *x,* where *x* is any digit between 0 and 9. ✓
Examples: 2421 code, 8421 code or XS3 code. ✓ (2)

2.2



(7)

2.3 2.3.1 60 to its binary XS3 equivalent.

6	0
↓	↓
0110	0000
+11	+11
1001 ✓	**0011** ✓

OR

6	0
+3	+3
9	3
↓	↓
1001 ✓	**0011** ✓

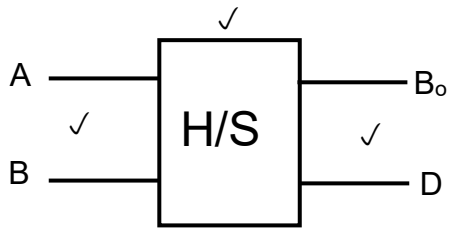
(2)

2.3.2 111100111100 2421 BCD code to its decimal equivalent.

2421	**2421**	**2421**
1111	0011	1100
↓✓	↓✓	↓✓
9	**3**	**6**

(3)

2.4 2.4.1



(3)

2.4.2

A	**B**	**D** ✓	**B_{out}** ✓
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

✓

(3)

2.5 2.5.1 $11111_2 - 11011_2$

	1	1	1	1	1
-	1	1	0	1	1
	0	**0**	**1**	**0**	**0** ✓

16	8	4	2	1
0	0	1	0	0

$\therefore 100_2 = 4 + 0 + 0 = 4_{10}$ ✓ ✓

(3)

2.5.2 $110_2 \times 1111_2$

				1	1	0		
		x	1	1	1	1		
				1	1	0		
			1	1	0	0	✓	
		1	1	0	0	0		
	1	1	0	0	0	0		
1	**0**	**1**	**1**	**0**	**1**	**0**	✓	

64	32	16	8	4	2	1
1	0	1	1	0	1	0

$\therefore 1011010_2 = 64 + 16 + 8 + 2$ ✓
$= 90_{10}$ ✓

(4)

2.6 2.6.1 $25_{10} + 31_{10} + 10_{10}$

	16	**8**	**4**	**2**	**1**	
25 =	1	1	0	0	1	✓
31 =	1	1	1	1	1	✓
10 =		1	0	1	0	✓

		1	**0**				
		1	1	0	0	1	
		1	1	1	1	1	
+			1	0	1	0	
1	**0**	**0**	**0**	**0**	**1**	**0**	✓

(4)

2.6.2 $120_{10} \div 15_{10}$

	64	**32**	**16**	**8**	**4**	**2**	**1**	
120 =	1	1	1	1	0	0	0	✓
15 =				1	1	1	1	✓

					1	0	0	0 ✓	
1	1	1	1	1	1	1	0	0	0
				1	1	1	1		
				0	0	0	0	0	
						0	0	0	0
					0	0	0	0	0
						0	0	0	0 ✓
						0	0	0	0

(4)
[35]

QUESTION 3

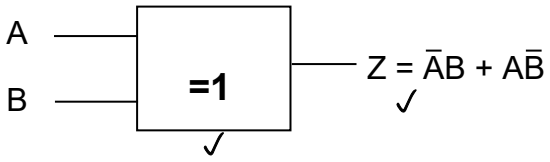
3.1 3.1.1 Gate **C** = AND-gate
Gate **D** = NAND-gate
Gate **E** = NOT-gate or Inverter (3 x 1) (3)

3.1.2

INPUTS		OUTPUTS		
A	**B**	**X**	**Y**	**Z**
0	0	0	1	0
1	1	0	1	0
1	0	0	1	0
0	1	1	0	1
		✓	✓	✓

(3)

3.2 3.2.1



✓ ✓

(2)

3.2.2

A	**B**	**Z**	
0	0	0	✓
0	1	0	
1	0	0	✓
1	1	1	✓

(3)

3.3

A	**B**	**Z**	
0	0	0	✓
0	1	0	
1	0	0	✓
1	1	1	✓

(4)

3.4 3.4.1 Clocked RS flip-flop. ✓ (1)

3.4.2 NAND gates (1)

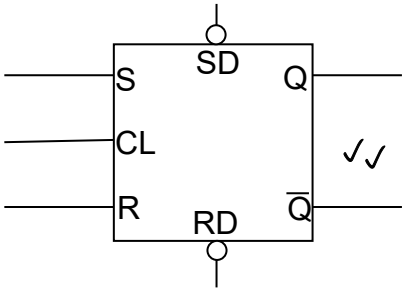
3.4.3 1 (1)

3.4.4

S	R	Q	$\overline{Q}$	
0	0	Q_n	Q_n	✓
0	1	0	1	✓
1	0	1	0	✓
1	1			✓

(4)

3.4.5



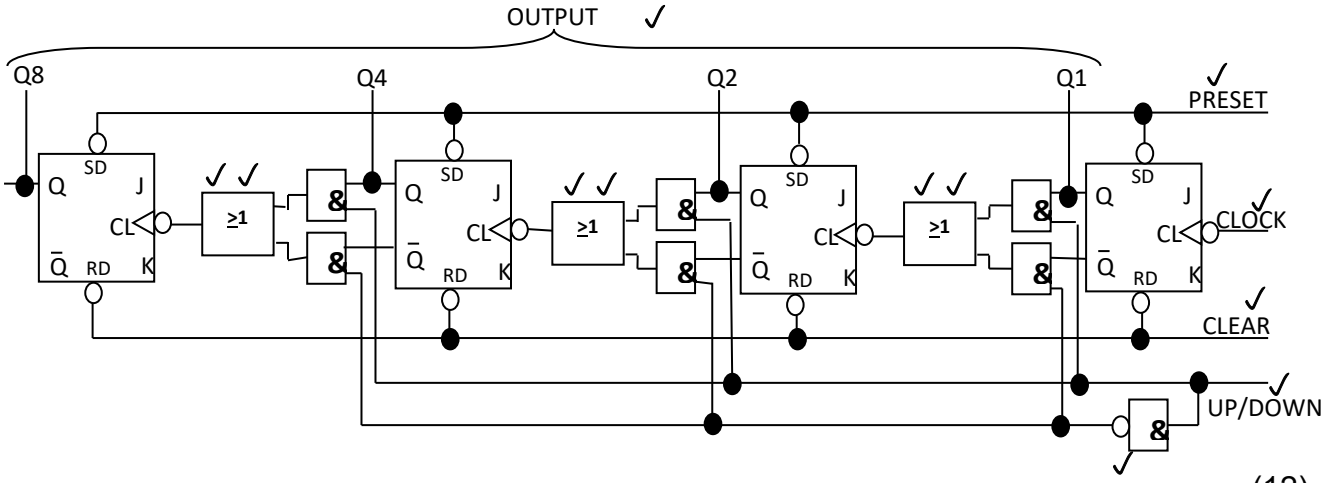
(2)

3.5 Compact Disk Re-Writable (1)

[25]

QUESTION 4

4.1



(12)

4.2

	✓	✓	✓	✓
Clock pulses	Q_8	Q_4	Q_2	Q_1
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0
10	1	0	0	1
11	1	0	0	0

(4)

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4.3
- Sequence generator
- Twisted ring counter
- Ring counter
- Delay line
- Parallel to serial converter
- Serial to parallel converter (Any 5 x 1) (5)

4.4 On a parallel-in parallel-out shift register the inputs are entered at the same time.
In a series-in parallel-out shift register the inputs are entered one at time.
(2 x 2) (4)
[25]

TOTAL: 100

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