higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T840(E)(A6)T

AUGUST EXAMINATION

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

6 August 2014 (Y-Paper)
13:00–16:00

Calculators may NOT be used.

This question paper consists of 6 pages.

ENGINEERING

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

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SECTION A

QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 A synchronous counter is made from:

A T-type flip-flop
B D-type flip-flop
C J-K flip-flop
D S-R flip-flop

1.1.2 A NOT gate added to an AND gate will give a/an:

A NOR gate
B NAND gate
C OR gate
D AND gate

1.1.3 1001 is the binary number for decimal:

A Eleven
B Nine
C Six
D Three

1.1.4 A four-bit shift register will store decimal numbers up to:

A Four
B Eight
C Ten
D Fifteen

1.1.5 An output of full adder is in the form of :

A Sum and carry
B Carry
C Sum
D Difference

(5 x 1) (5)

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1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

1.2.1 Another term used to describe up/down counters is bidirectional.

1.2.2 The output of an exclusive-OR (XOR) gate is 1 only when the inputs are different.

1.2.3 An output of a NOT gate is a complement of its input.

1.2.4 When using the excess-three code a value of 3 is subtracted from each column of a decimal digit before it is converted to a 4-bit binary code.

1.2.5 A D-type flip-flop is constructed by connecting an inverter between the set and the clock terminals.

(5 x 1) (5)
[10]

TOTAL SECTION A: 10

SECTION B

QUESTION 2

2.1 Give FOUR binary multiplication rules. (4)

2.2 Calculate the following numbers in binary number systems and convert the final answer to a decimal number system:

2.2.1 10101 + 100010 +1101 (4)

2.2.2 110010 ÷ 1010 (4)

2.3 Convert each of the following decimal numbers to their binary equivalents and then complete the calculations in the binary number system:

2.3.1 47 - 24 (4)

2.3.2 11 x 14 (6)

2.4 Draw a fully labelled logic circuit diagram of a half subtractor making use of AND, XOR and NOT gates, and also draw its IEC symbol. (7)

2.5 Convert the following numbers to the code as indicated:

2.5.1 196 decimal to its 2421 BCD code. (3)

2.5.2 110010010110 XS3 to its decimal equivalent. (3)

2.6 Draw the truth table of an 8421 decoder. (5)
[40]

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QUESTION 3

3.1 Study the switch circuits in TABLE 1 below and answer the questions:

INPUTS		OUTPUTS		
A	B	X	Y	Z
0	0	0	1	1
1	1	0	0	0
0	1	1	1	0
1	0	1	1	0

TABLE 1

3.1.1 Name the gates represented by output X, Y and Z. (3)

3.1.2 Draw the IEC symbol for the gate represented by output Y. (3)

3.1.3 Draw the switch circuit for the gate represented by output X. (4)

3.1.4 Define the gate represented by output Z. (2)

3.2 Study FIGURE 1 below and answer the questions:

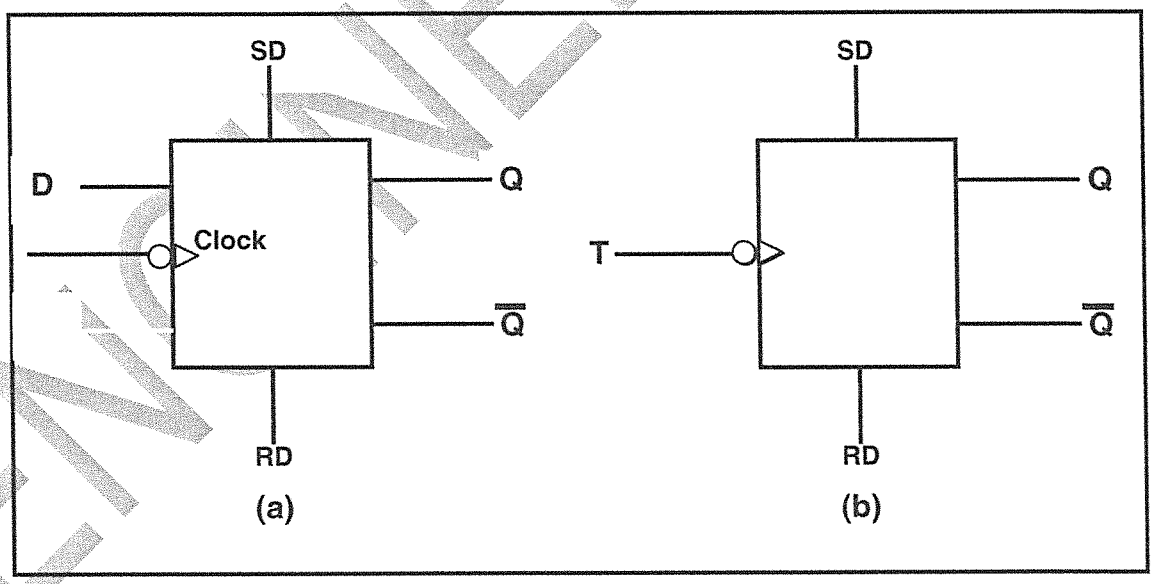


FIGURE 1

3.2.1 What types of flip-flops are represented by the two IEC symbols in FIGURE 1 above? (2)

3.2.2 Draw the truth table for the flip-flop in FIGURE 1(a) above. (2)

3.2.3 What is the meaning of the circle and triangle on the clock input of the flip-flop in FIGURE 1(a) or FIGURE 1(b) above? (4)

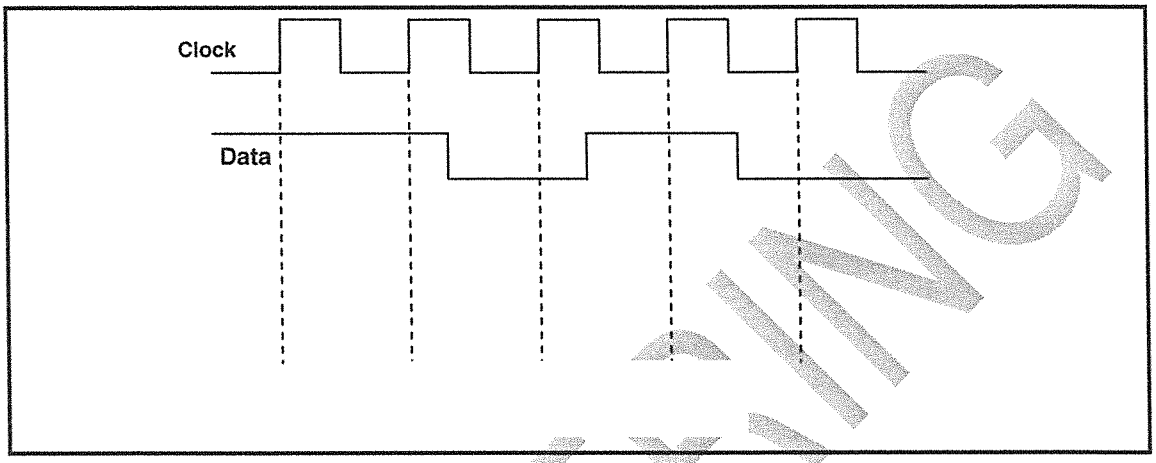
3.3 Draw a labelled hysteresis loop. (5)

[25]

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QUESTION 4

4.1 By making use of a 3-bit shift register, redraw and complete the following timing diagram in FIGURE 2 below. Assume that the register is initially cleared (all 0s).



(6)

FIGURE 2

4.2 Draw a fully labelled circuit diagram of a shift register using D-type flip-flops with the following features: series input, series output. (6)

4.3 What is an asynchronous counter? (2)

4.4 Draw a neat labelled circuit diagram of an asynchronous binary-down single JK-type flip-flop, and also draw its truth table. (11)
[25]

TOTAL SECTION B: 90

GRAND TOTAL: 100

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