higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

AUGUST EXAMINATION

LOGIC SYSTEMS N2

6 AUGUST 2014

This marking guideline consists of 7 pages.

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SECTION A

QUESTION 1

1.1
1.1.1 C✓
1.1.2 B✓
1.1.3 B✓
1.1.4 E ✓
1.1.5 A ✓

(5 x 1) (5)

1.2
1.2.1 True✓
1.2.2 True✓
1.2.3 True✓
1.2.4 False✓
1.2.5 False✓

(5 x 1) (5)
[10]

TOTAL SECTION A: 10

SECTION B

QUESTION 2

2.1
1 x 1 = 1✓
1 x 0 = 0✓
0 x 1 = 0✓
0 x 0 = 0✓

(4)

2.2 2.2.1

		1	0	1	0	1
	1	0	0	0	1	0
+			1	1	0	1
1	**0**	**0**	**0**	**1**	**0**	**0** ✓✓

64	32	16	8	4	2	1
1	**0**	**0**	**0**	**1**	**0**	**0**

$\therefore 101010_2 = 64 + 4✓ = 68_{10}$ ✓

(4)

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2.2.2

							1	0	1	✓
1	0	1	0	1	1	0	0	1	0	
				1	0	1	0			
				0	0	1	0	1		✓
					0	0	0	0		
					0	1	0	1	0	
						1	0	1	0	✓
						0	0	0	0	

8	4	2	1
0	1	0	1

$\therefore 101_2 = 5$ ✓

(4)

2.3 2.3.1

	32	16	8	4	2	1	
47 =	1	0	1	1	1	1	✓
24 =		1	1	0	0	0	✓

	1	0	1	1	1	1	
-		1	1	0	0	0	
		1	**0**	**1**	**1**	**1**	✓✓

(4)

2.3.2

	8	4	2	1	
11 =	1	0	1	1	✓
14 =	1	1	1	0	✓

				1	0	1	1	
			x	1	1	1	0	
				0	0	0	0	
			1	0	1	1		✓
		1	0	1	1			
	1	0	1	1				✓
1	**0**	**0**	**1**	**1**	**0**	**1**	**0**	✓✓

(6)

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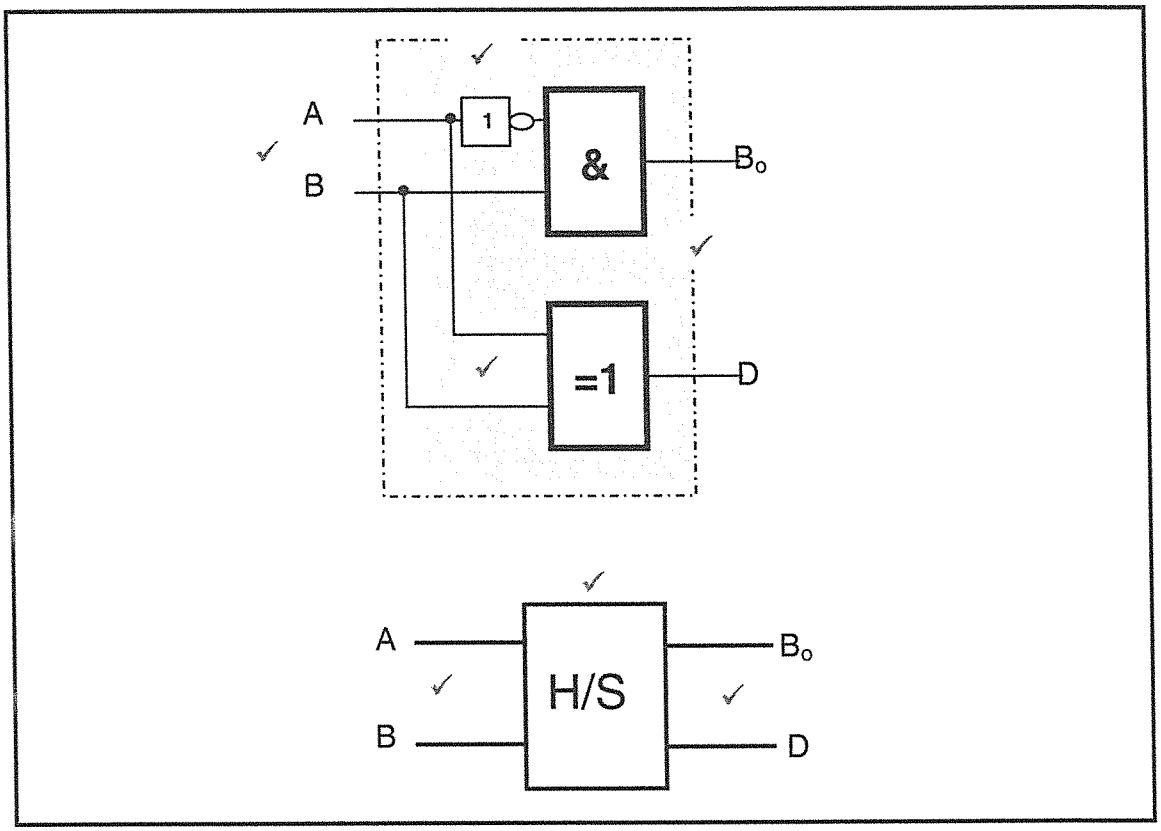
2.4



(7)

2.5 2.5.1

2421	2421	2421
1	9	6
↓✓	↓✓	↓✓
0001	1111	1100

(3)

2.5.2

1100	1001	0110
-11	-11	-11
1001	0110	0011
↓	↓	↓
9✓	6✓	3✓

OR

1100	1001	0110
↓	↓	↓
12	9	6
-3	-3	-3
9✓	6✓	3✓

(3)

2.6

BINARY INPUTS				DECIMAL OUTPUTS
8✓	4✓	2✓	1✓	✓
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

(5)
[40]

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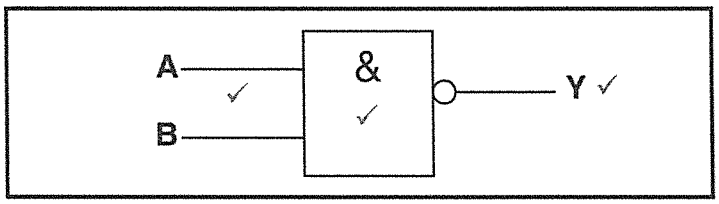
QUESTION 3

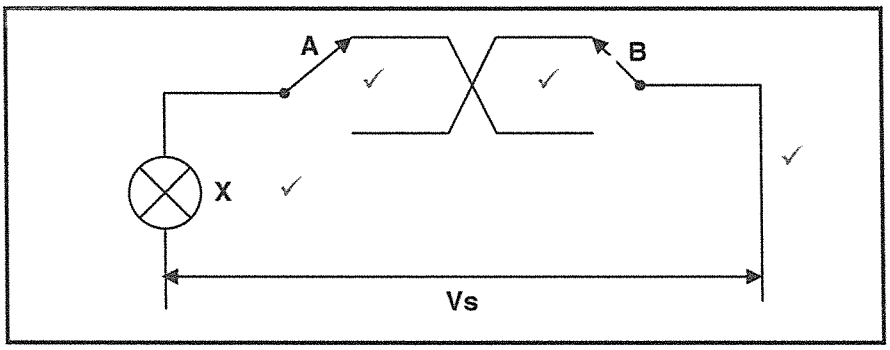
3.1 3.1.1 Output X is an XOR gate✓,
Output Y is a NAND gate✓ and
Output Z is a NOR gate. ✓ (3)

3.1.2



(3)

3.1.3



(4)

3.1.4 An output of a NOR gate will be logic 1 when all the inputs are logic zero otherwise it will be logic zero. ✓✓

OR

An output of a NOR gate will be logic 0 if any of the inputs is logic 1 otherwise it will be logic 1. (2)

3.2 3.2.1 Figure 1(a) is a clocked D-type master slave flip-flop ✓
Figure 1(b) is a clocked T-type master slave flip-flop ✓ (2)

3.2.2

CLOCK	D	Q	$\overline{Q}$
↑	0	Q_n	$\overline{Q_n}$
↑	1	1	0

✓
✓

(2)

3.2.3 The small triangle at the clock input depicts positive-edge triggering, ✓✓and the circle symbol represents negative-edge triggered. ✓✓ (4)

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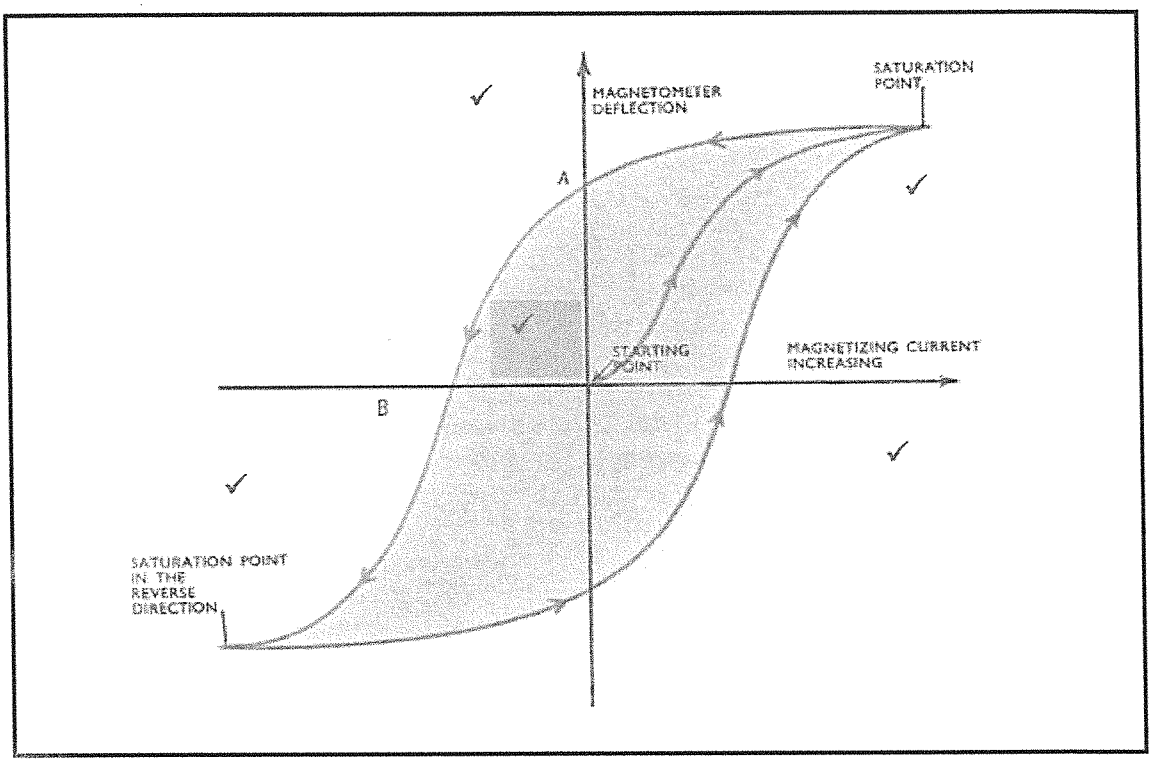
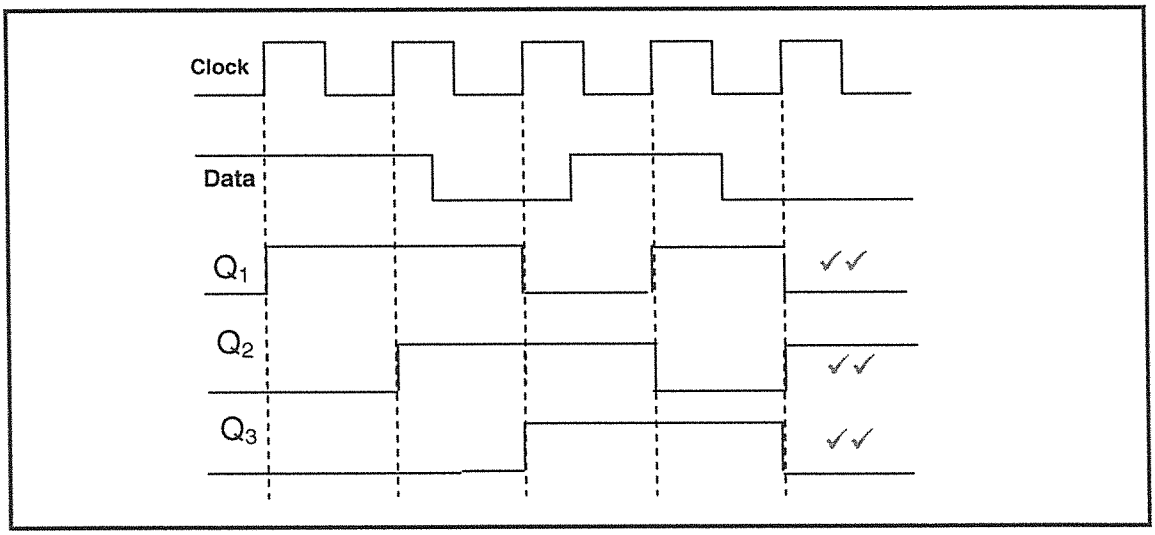
3.3



(5)
[25]

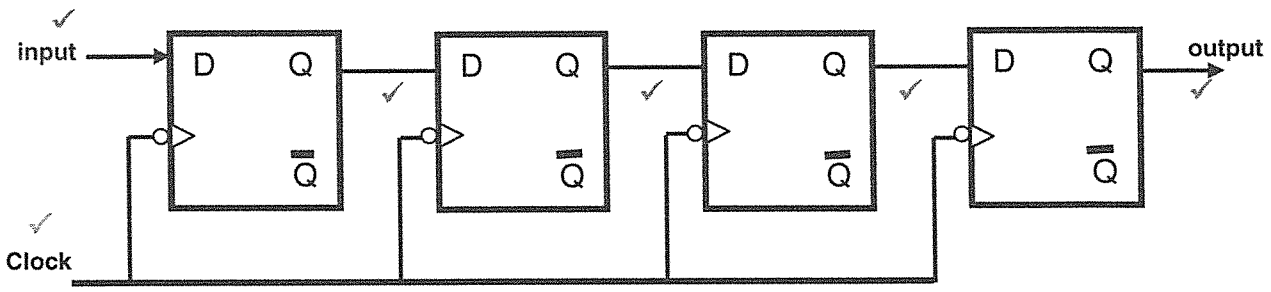
QUESTION 4

4.1



(6)

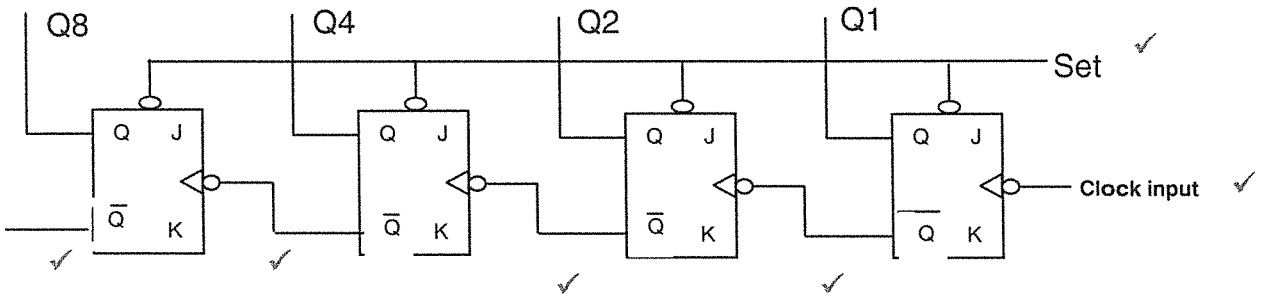
4.2



(6)

4.3 An asynchronous counter is a counter whereby only the first flip-flop is clocked by an external clock. ✓✓ (2)

4.4



CLOCK PULSES	Q_8 ✓	Q_4 ✓	Q_2 ✓	Q_1 ✓
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0
10	1	0	0	1
11	1	0	0	0

(11)
[25]

TOTAL SECTION B: 90

GRAND TOTAL: 100

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