higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N2

4 APRIL 2016

This marking guideline consists of 7 pages.

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QUESTION 1

1.1 1.1.1 $Y = 15_{10}$

	8	4	2	1
15 =	**1**	**1**	**1**	**1**

$\therefore Y = 15_{10} = 1111_2$✓

		1	0	1	1	0	1
				1	1	1	1
+				1	1	1	0
1	**0**✓	**0**	**1**	**0**✓	**1**	**0**	✓

(4)

1.1.2

64	32	16	8	4	2	1
1	**0**	**0**	**1**	**0**	**1**	**0**

$\therefore 101010_2 = 64 + 8 + 2$✓
$= 74_{10}$✓

(2)

1.1.3

								1	1✓
1	1	1	1	1	0	1	1	0	1
					1	1	1	1	
					0	1	1	1	1✓
						1	1	1	1
						0	0	0	0✓

8	**4**	**2**	**1**
0	0	1	1

$\therefore 11_2 = 2 + 1$ ✓$= 3_{10}$✓

(5)

1.1.4

				1	1	1	0	
			x	1	1	1	1	
				1	1	1	0	
			1	1	1	0		✓
		1	1	1	0			
	1	1	1	0				✓
1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	✓✓

(4)

1.1.5

	1	0	1	1	0	1	
-			1	1	1	0	
		1	**1**	**1**	**1**	**1**	✓✓

16	**8**	**4**	**2**	**1**
1	1	1	1	1

$\therefore 11111_2 = 16 + 8 + 4 + 2 + 1$✓
$= 31_{10}$✓ (4)

1.2 1.2.1 Full adder (2)

1.2.2

INPUTS			**OUTPUTS**		
A	**B**	**C_{in}**	**Sum**	**C_{out}**	
0	0	0	0	0	✓
0	0	1	1	0	
0	1	0	1	0	✓
0	1	1	0	1	
1	0	0	1	0	✓
1	0	1	0	1	
1	1	0	0	1	✓
1	1	1	1	1	

(4)
[25]

QUESTION 2

2.1 FOUR logic gates (2)

2.2 2.2.1 Encoder converts decimal code to binary code.✓✓

2.2.2 Decoder converts binary code to decimal code.✓✓ (2 x 2) (4)

2.3 2.3.1

7421	**7421**	**7421**
1	**5**	**8**
↓✓	↓✓	↓✓
0001	0101	1001

2.3.2

2421	**2421**	**2421**
0011	1100	1111
↓✓	↓✓	↓✓
3	**6**	**9**

2.3.3

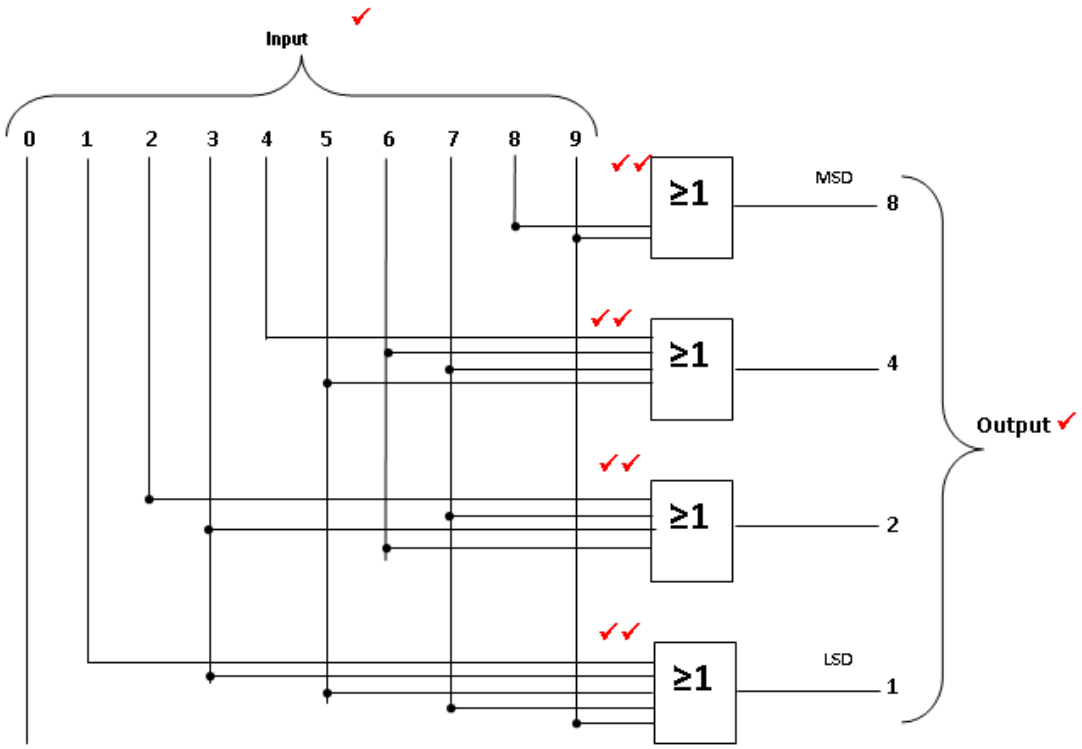
1 + 0 + 0 + 1 + 0 + 1

✓ ↓ ↓ ↓ ↓ ↓ ↓

1 1 0 1 1 1 ✓

∴The binary of 100101_2 is 11 0111 $_{Grey}$ ✓ (3 x 3) (9)

2.4



(10)

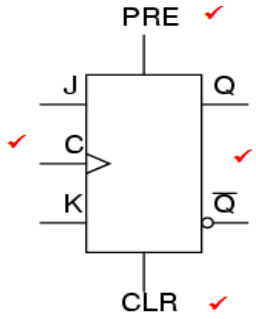
[25]

QUESTION 3

3.1 3.1.1 When the PRESET input is active (PRE = 1), the output of the flip-flop is forced to 1 immediately.

3.1.2 When the CLEAR signal is active (i.e., CLR = 0), the output of the flip- flop is forced to 0 immediately. (2 x 2) (4)

3.2



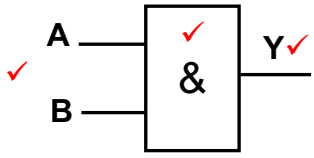
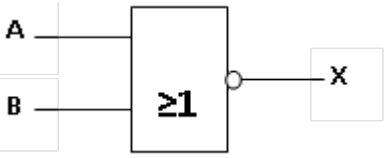
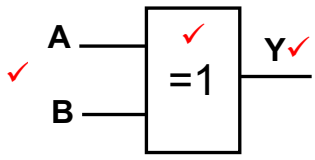
(4)

3.3

- Speed
- Capacity
- Cost
- Convenience/Inconvenience
- Type of memory

(5)

3.4

LOGIC GATE NAME	IEC SYMBOL	TRUTH TABLE
AND		A B Z 0 0 0 0 1 0 1 0 0 1 1 1
NOR		A B Z 0 0 1 0 1 0 1 0 0 1 1 0
XOR		A B Z 0 0 0 0 1 1 1 0 1 1 1 0

(12)
[25]

QUESTION 4

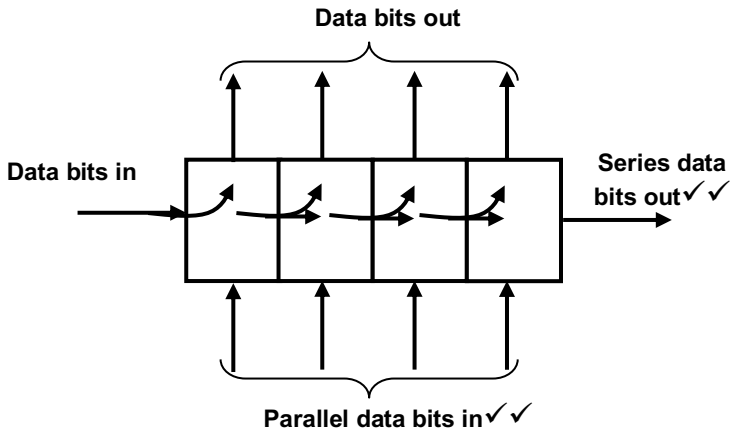
4.1
- Serial to parallel converter✓
- Parallel to serial converter✓
- Delay line✓
- Ring counter✓
- Twisted-ring counter
- Sequence generator

(Any 4 x 1) (4)

4.2 FOUR flip-flops (2)

4.3 4.3.1 Series-in parallel-out shift register. (2)

4.3.2



(4)

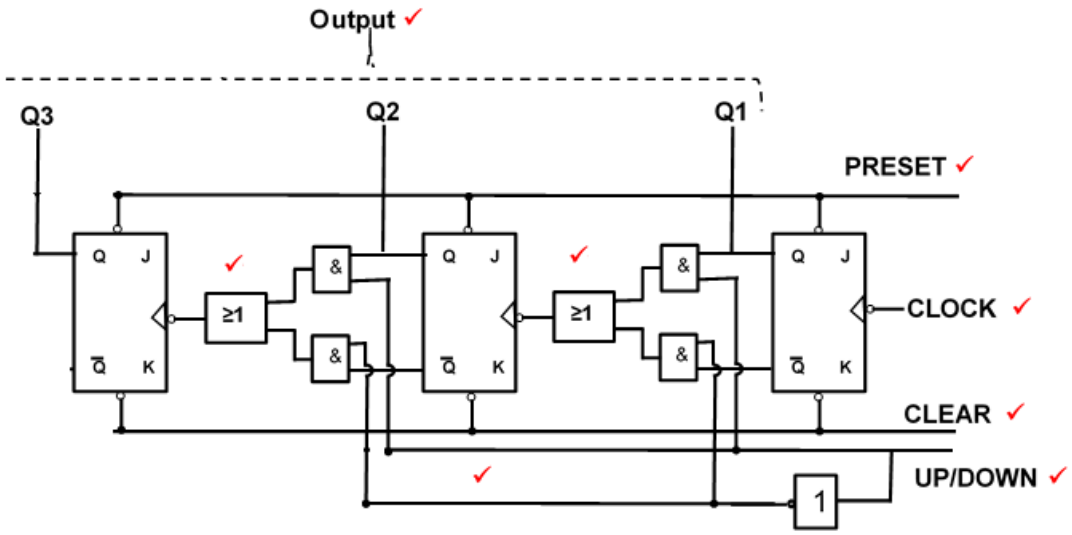
4.4

	✓	✓	✓	✓
Clock pulses	Q_8	Q_4	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

✓(correctness)

(5)

4.5



(8)
[25]

TOTAL: 100

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