higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

APRIL EXAMINATION

LOGIC SYSTEMS N2

15 APRIL 2015

This marking guideline consists of 8 pages.

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SECTION A

QUESTION 1

1.1	1.1.1	B
	1.1.2	C
	1.1.3	A
	1.1.4	A
	1.1.5	C

(5 × 1) (5)

1.2	1.2.1	False
	1.2.2	True
	1.2.3	True
	1.2.4	False
	1.2.5	True

(5 × 1) (5)
[10]

TOTAL SECTION A: 10

SECTION B

QUESTION 2

2.1 2.1.1

	8	4	2	1	
8 =	1	0	0	0	✓

```
                        1   0   0   1✓
1   0   0   0 | 1   0   0   1   0   0   0
                1   0   0   0
                0   0   0   1           ✓
                    0   0   0   0
                    0   0   1   0   0
                        0   0   0   0   0✓
                        0   1   0   0   0
```

8	4	2	1
0	1	1	0

$\therefore 1010_2 = 8 + 2 = 10_{10}$ ✓ (5)

2.1.2

	8	**4**	**2**	**1**	
13 =	1	1	0	1	✓

				1	1	1	0		
			x	1	1	0	1		
				1	1	1	0		
			0	0	0	0			✓✓
		1	1	0	1				
	1	1	0	1					
1	**0**	**1**	**0**	**1**	**0**	**1**	**0**		✓

(4)

2.1.3

	16	**8**	**4**	**2**	**1**	
27 =	1	1	0	1	1	✓

	1	1	1	0	1	0	
-		1	1	0	1	1	
	1	**1**	**1**	**1**	**1**		✓✓

16	8	4	2	1
1	1	1	1	1

$\therefore 11011_2 = 16 + 8 + 4 + 2 + 1 = 31_{10}$ ✓

(4)

2.1.4 $17_{10} + 21_{10} + 1011_2$

	16	**8**	**4**	**2**	**1**	
17 =	1	0	0	0	1	✓
21 =	1	0	1	0	1	✓

		1	0	0	0	1	
		1	0	1	0	1	
+			1	0	1	1	
	1	**1**	**0**	**0**	**0**	**1**	✓✓

(4)

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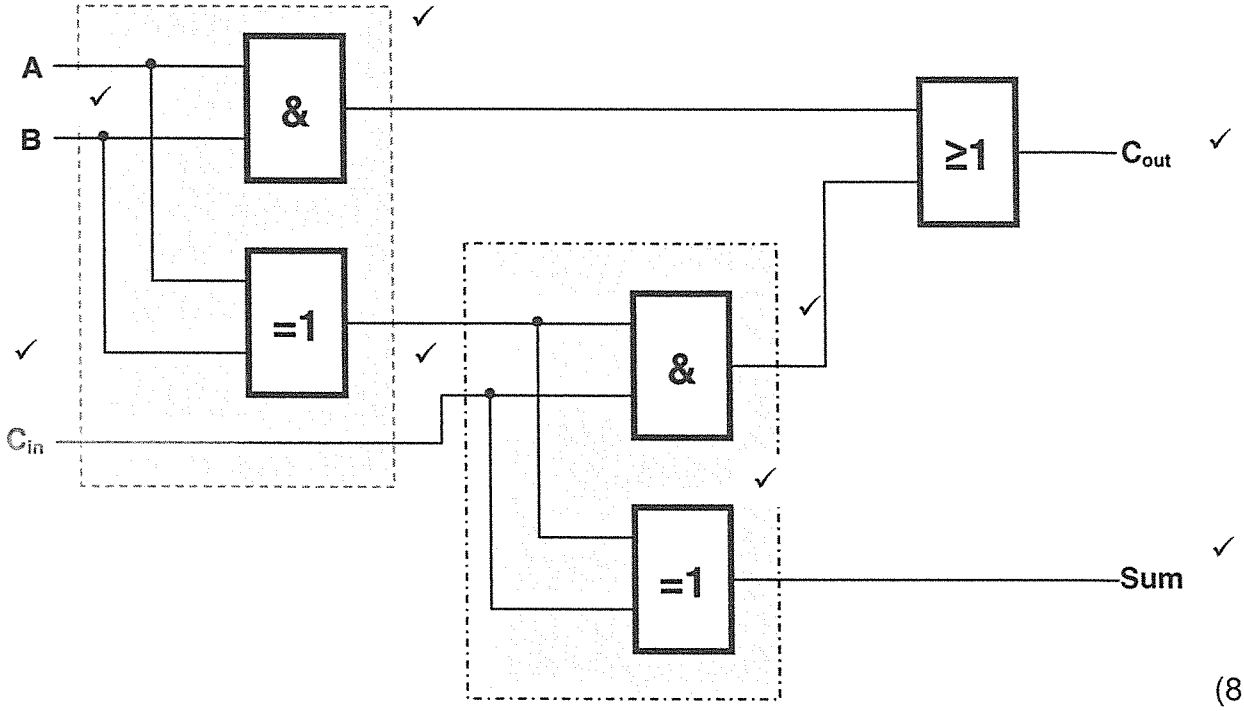
2.2



(8)

2.3 2.3.1

8421	8421	8421
1000	1001	0111
↓✓	↓✓	↓✓
8	9	7

(3)

2.3.2

1000	1001	0111
-11	-11	-11
0101	0110	0100
↓	↓	↓
5✓	6✓	4✓

OR

1000	1001	0111
↓	↓	↓
8	9	7
-3	-3	-3
5✓	6✓	4✓

(3)

2.4
2.4.1 Decimal
2.4.2 Binary
2.4.3 Shift register
2.4.4 Clock
2.4.5 Stored
2.4.6 Shift register
2.4.7 Clock pulse
2.4.8 Binary
2.4.9 Seven

(9 × 1) (9)
[40]

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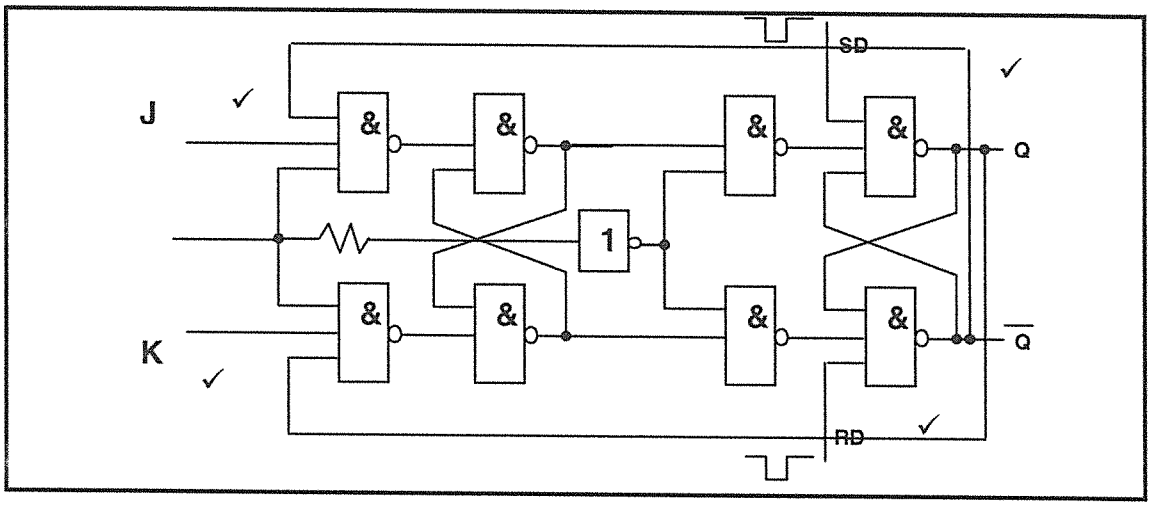
QUESTION 3

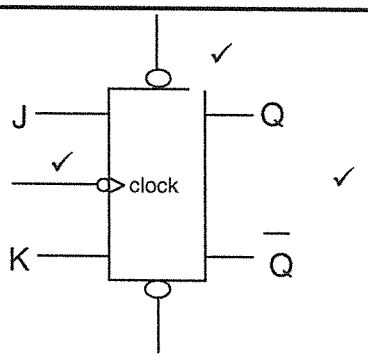
3.1.1



(4)

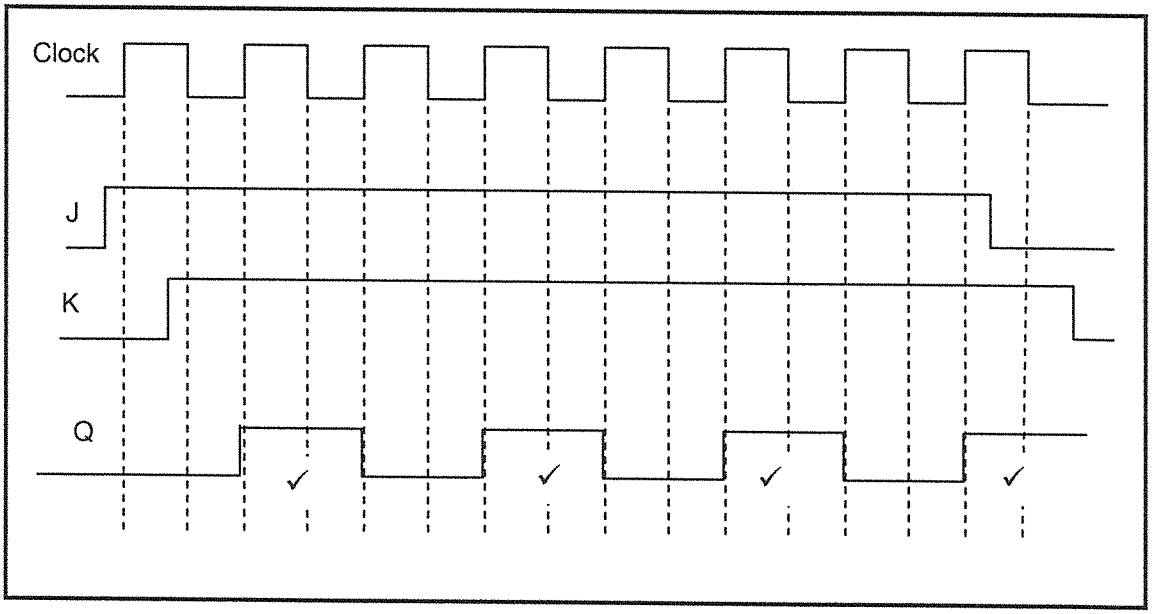
3.1.2

J	K	✓ Q	✓ $\overline{Q}$
0	0	Qn	$\overline{Q}$n
0	1	0	1
1	0	1	0
1	1	$\overline{Q}$n	Qn



(5)

3.2



(4)

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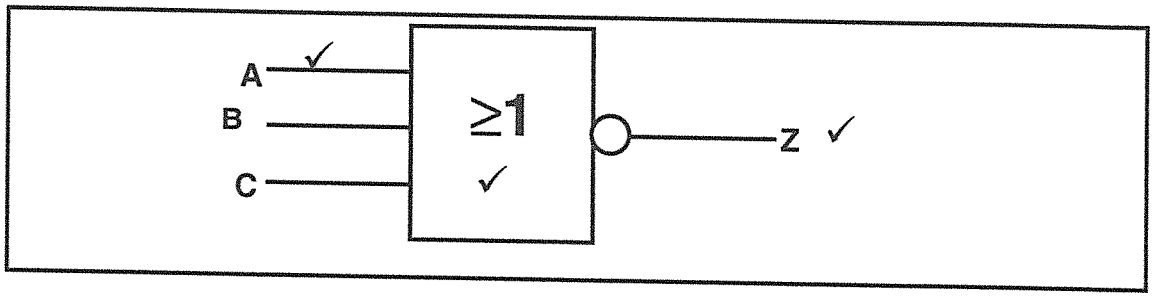
3.3

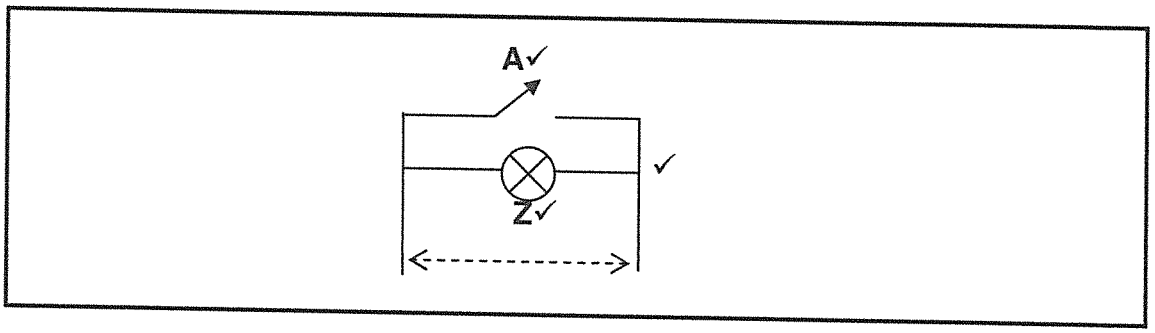


(3)

3.4 An out of NAND gate will be logic 0 when all the inputs are logic 1, otherwise it will be logi 1.✓✓

(2)

3.5



(3)

3.6 Main memory✓

(1)

Example:
- Magnetic core✓
- Semiconductor memory

(Any 1 × 1) (1)

Secondary memory✓

(1)

Example:
- CD
- DVD
- Floppy
- Magnetic tape
- Flash drive

(Any 1 × 1) (1)

[25]

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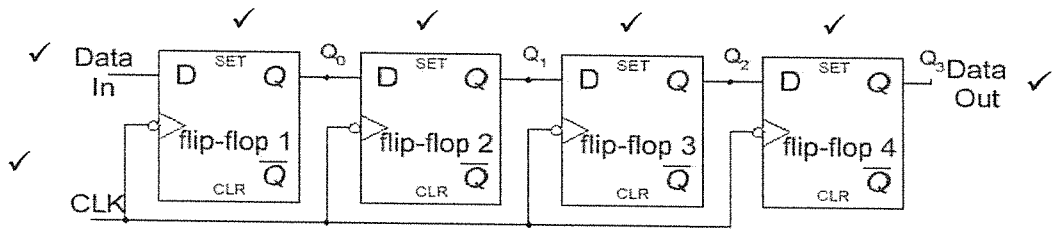
QUESTION 4

4.1 The output of SISO is in series✓✓ while the output of SIPO is in parallel.✓✓ (4)

4.2



(7)

4.3

Clock pulses	✓	✓	✓	✓
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0
11	0	0	0	1

✓ (For correctness)

(5)

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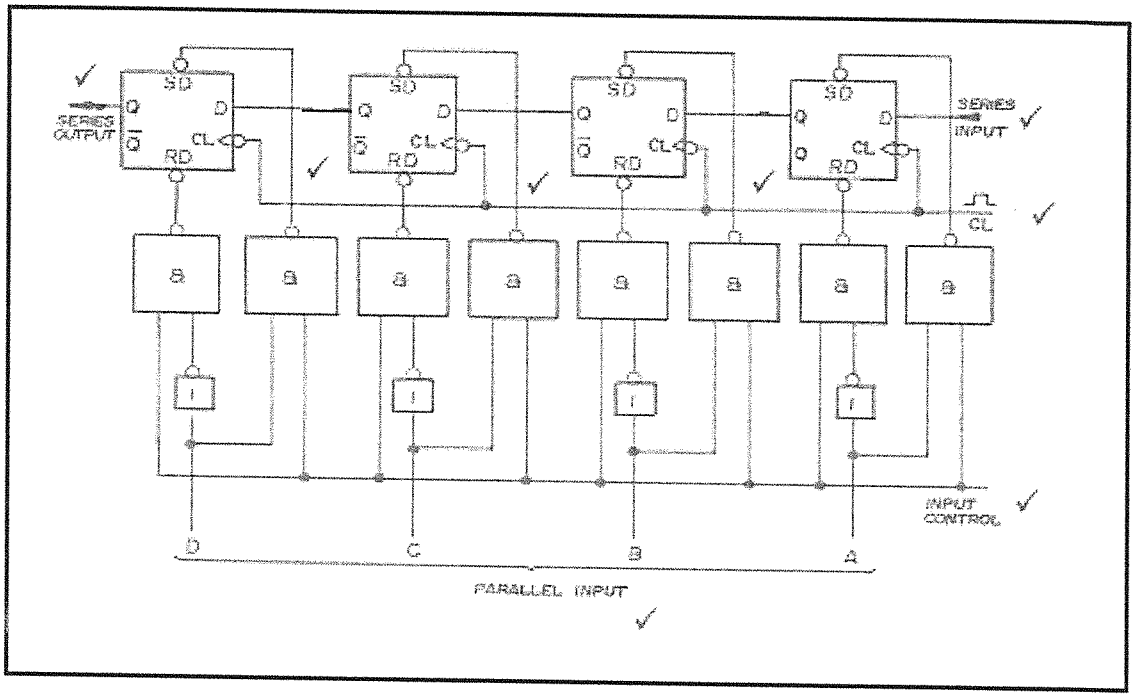
4.4



(9)
[25]

TOTAL SECTION B: 90
GRAND TOTAL: 100

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