higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

T860(E)(A15)T

# APRIL EXAMINATION

# NATIONAL CERTIFICATE

# LOGIC SYSTEMS N2

(8080262)

**15 April 2015 (Y-Paper)**
**13:00–16:00**

**Calculators may NOT be used.**

**This question paper consists of 6 pages.**

ENGINEERING

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# DEPARTMENT OF HIGHER EDUCATION AND TRAINING
# REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

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**INSTRUCTIONS AND INFORMATION**

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Write neatly and legibly.

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## SECTION A

## QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 Select the statement that best describes Read-Only Memory (ROM).

A Non-volatile, used to store information that changes during system operation.
B Non-volatile, used to store information that does not change during system operation.
C Volatile, used to store information that changes during system operation.
D Volatile, used to store information that does not change during system operation.

1.1.2 What input values will cause an AND logic gate to produce a HIGH output?

A At least one input is HIGH
B At least one input is LOW
C All inputs are HIGH
D All inputs are LOW

1.1.3 The binary equivalent of $16_{10}$ is equal to …

A 10000.
B 11000.
C 01100.
D 10100.

1.1.4 How many flip-flops are required to produce a FOUR-bit shift register?

A 4
B 8
C 10
D 15

1.1.5 A full adder can be made up of …

A two half adders.
B two half adders and a NOR gate.
C two half adders and an OR gate.
D two half adders and an AND gate.

(5 × 1) (5)

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1.2 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

1.2.1 Asynchronous inputs will cause the flip-flop to respond immediately with regard to the clock input.

1.2.2 An output of an exclusive-OR (XOR) gate is 1 only when the inputs are different.

1.2.3 Decimal numbers can be converted into binary by dividing by two and recording the remainders.

1.2.4 Two half adders can be combined to form a full adder with no additional gates.

1.2.5 A parallel-in, serial-out shift register enters all data bits simultaneously and transfers them out one bit at a time.

(5 × 1) (5)
**[10]**

**TOTAL SECTION A: 10**

## SECTION B

## QUESTION 2

2.1 Convert each of the following numbers to their binary equivalents and then complete the calculation in the binary number system:

2.1.1 $1001000_2 \div 8_{10}$ [convert the answer to the decimal number system] (5)

2.1.2 $13_{10} \times 1110_2$ (4)

2.1.3 $111010_2 - 27_{10}$ [convert the answer to the decimal number system] (4)

2.1.4 $17_{10} + 21_{10} + 1011_2$ (4)

2.2 Draw a fully labelled logic circuit diagram of a full adder using AND, XOR and OR gates. (8)

2.3 Convert the following numbers to the code as indicated:

2.3.1 100100110110 8421 BCD code to its decimal equivalent. (3)

2.3.2 100100110110 XS3 to its decimal equivalent. (3)

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2.4 Complete the following sentences by filling in the missing word(s). Write only the word(s) next to the question number (2.4.1–2.4.9) in the ANSWER BOOK.

The encoder changes the (2.4.1 ...) input to a (2.4.2 ...) code, which is passed to the (2.4.3 ...) during a (2.4.4 ...) pulse. It is (2.4.5 ...) in the (2.4.6 ...) until another (2.4.7 ...) is applied. The decoder converts the (2.4.8 ...) code into a (2.4.9 ...) segment display code. (9 × 1) (9)

**[40]**

## QUESTION 3

3.1 Study FIGURE 1 below and answer the questions.

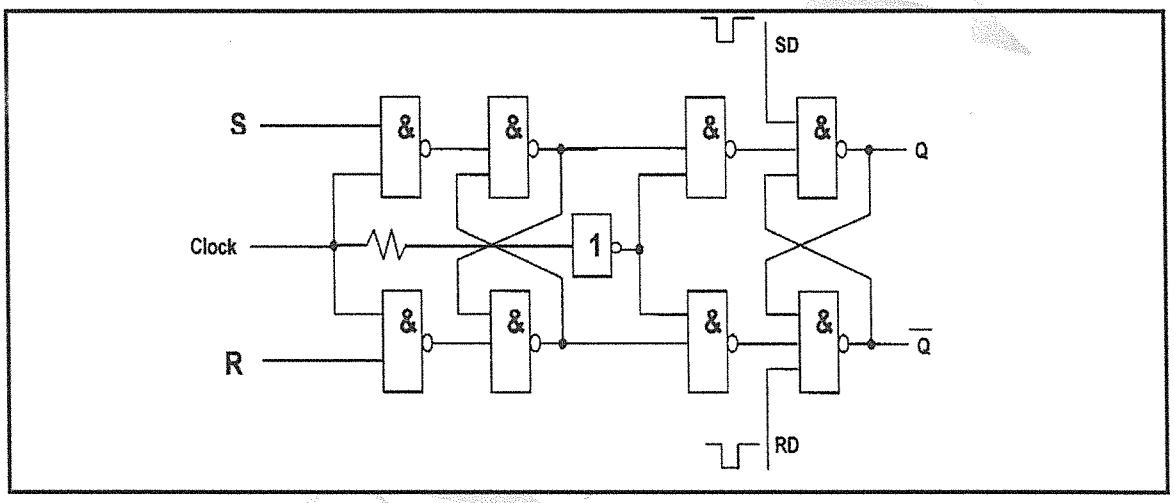



**FIGURE 1**

3.1.1 Show how FIGURE 1 above can be converted to a JK master-slave flip-flop. (4)

3.1.2 Draw the truth table and also the IEC symbol for the flip-flop in QUESTION 3.1.1 above. (5)

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3.2 For a positive edge-triggered J-K flip-flop with inputs as shown in FIGURE 2 below, draw the corresponding output waveform Q. Assume Q starts low.

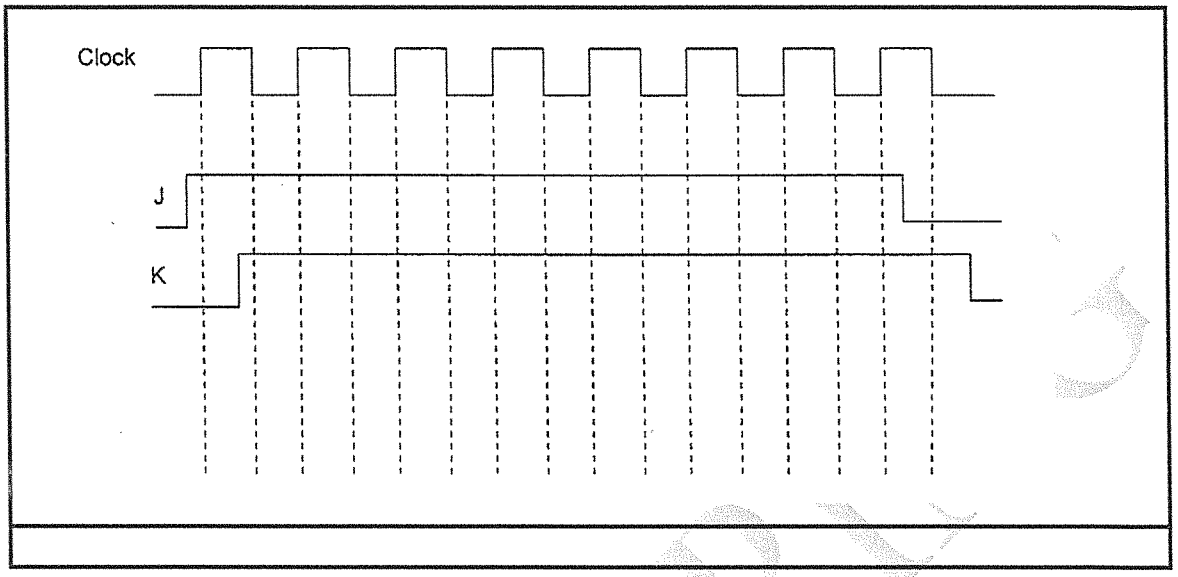



**FIGURE 2** (4)

3.3 Draw an IEC symbol for a THREE-input NOR gate. (3)

3.4 Define *NAND gate.* (2)

3.5 Draw the switch circuit for a NOT gate. (3)

3.6 Name TWO groups of memories and give ONE example of each group. (4)
**[25]**

**QUESTION 4**

4.1 What is the difference between a series-in series-out shift register and a series-in parallel-out shift register? (4)

4.2 Draw a fully labelled circuit diagram of a right shift register using D-type flip-flops with the following features: series input, parallel output and series output. (7)

4.3 Draw the truth table of a FOUR-bit decade up-counter. (5)

4.4 Draw a fully labelled circuit diagram of a right-shift register using D-type flip-flops with the following features: parallel input, series. (9)
**[25]**

**TOTAL SECTION B: 90**
**GRAND TOTAL: 100**

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