higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

# MARKING GUIDELINE

## NATIONAL CERTIFICATE

## DIGITAL ELECTRONICS N5

**19 November 2020**

**This marking guideline consists of 7 pages.**

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## QUESTION 1

1.1

E6, $F_{16} \div 43,5_8$

$E6,F_{16} = 11100110,1111_2$ √

$43,5_8 = 100011,101_2$ √

∴ E6, $F_{16} \div 43,5_8 = 11100110,1111_2 \div 100011,101_2$

$11100110,1111_2 \div 100011,101_2$

```
                    1 1 0 , 0 1 1 1√
1 0 0 0 1 1 1 0 1 0 √1 1 1 0 0 1 1 0 1 1 1 1 ,0 0 0 0
                  1 0 0 0 1 1 1 0 1 0
                    1 0 1 1 0 0 0 0 1 1
                    1 0 0 0 1 1 1 0 1 0
                    1 0 0 0 1 0 0 1 1 0 0        √
                      1 0 0 0 1 1 1 0 1 0
                      1 0 0 0 0 1 0 0 1 0 0
                       1 0 0 0 1 1 1 0 1 0
                         1 1 1 1 0 1 0 1 0 0
                         1 0 0 0 1 1 1 0 1 0 ✓
                           1 1 0 0 1 1 0 1 0✓
```

∴ $11100110,1\ 111_2 \div 100011,101_2 = 110,0111_2$ rem $\frac{110011010}{1000111010}$ √

$110,0111_2 = 6,7_{16}$√ (6)

1.2

$96,E_{16} = 10010110,\ 1110_2$
$= 10010110,111_2$ √

$53,2_8 = 101011,010_2$
$= 101011,01_2$ √

```
                                  1 0 0 1 0 1 1 0 1 1 1
                                        1 0 1 0 1 1 0 1
                                  1 0 0 1 0 1 1 0 1 1 1
                                1 0 0 1 0 1 1 0 1 1 1 0 0   √
                              1 0 0 1 0 1 1 0 1 1 1 0 0 0
                            1 0 0 1 0 1 1 0 1 1 10 0 0 0 0√
                          1 0 0 1 0 1 1 0 1 1 10 0 0 0 0 0 0
                        1 1 0 0 1 0 1 1 1 1 1 0 1 0 1 0 1 1√
```

∴$96,E_{16} \times 53,2_8 = 10010110,111_2 \times 101011,01_2$

∴$10010110,111_2 \times 101011,01_2 = 1100101111101,01011_2 = 14575,26_8$√ (6)

1.3 $122,3_8 = 001\ 010\ 010\ ,\ 011_2$
$= 1010010,011_2$✓

$122,B_{16} = 0001\ 0010\ 0010,\ 1011_2$
$= 100100010,1011_2$
$= 100100010,101_2$✓

$\therefore 1221,3_8 - 122,B_{16} = 1010010,011_2 - 100100010,101_2$

001010010,011
100100010,101 ⟶ 011011101,010 +1
No Carry

0 0 1 0 1 0 0 1 0 , 0 1 1
0 1 1 0 1 1 1 0 1 , 0 1 1✓
1 0 0 1 0 1 1 1 1 , 1 1 0

*∴ the answer is negative, compleemnt the answer*

0 1 1 0 1 0 0 0 0 , 0 0 1
+1✓
- 0 1 1 0 1 0 0 0 0 , 0 1 0

$\therefore 1010010,011_2 - 100100010,101_2 = -\ 11010000,010_2$✓
$= -\ 208,25_{10}$✓

(6)
**[18]**

## QUESTION 2

| A | B | C | D | | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ | $J_D$ | $K_D$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | 0 | X | 0 | X | 0 | X | 1 | 1 | ✓ |
| 0 | 0 | 0 | 1 | | 0 | X | 0 | X | 1 | X | X | X | ✓ |
| 0 | 0 | 1 | 0 | | 0 | X | 0 | X | X | 0 | 1 | 1 | ✓ |
| 0 | 0 | 1 | 1 | | 0 | X | 1 | X | X | 1 | X | X | ✓ |
| 0 | 1 | 0 | 0 | | 0 | X | X | 0 | 0 | X | 1 | 1 | |
| 0 | 1 | 0 | 1 | | 0 | X | X | 0 | 1 | X | X | X | ✓ |
| 0 | 1 | 1 | 0 | | 0 | X | X | 0 | X | 0 | 1 | 1 | ✓ |
| 0 | 1 | 1 | 1 | | 1 | X | X | 1 | X | 1 | X | X | ✓ |
| 1 | 0 | 0 | 0 | | X | 0 | 0 | X | 0 | X | 1 | 1 | ✓ |
| 1 | 0 | 0 | 1 | | X | 1 | 0 | X | 0 | X | X | X | ✓ |

1010
1011
1100
1101
1110

Don't cares (X's) ✓

(10)

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | 0 | 0 | d | d |
| $\overline{C}D$ | 0 | 0 | d | d |
| $CD$ | 0 | 1 | d | d |
| $C\overline{D}$ | 0 | 0 | d | d |

$Ja = BCD$ ✓

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | d | d | d | 0 |
| $\overline{C}D$ | d | d | d | 1 |
| $CD$ | d | d | d | d |
| $C\overline{D}$ | d | d | d | d |

$Ka = D$ ✓

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | 0 | d | d | 0 |
| $\overline{C}D$ | 0 | d | d | 0 |
| $CD$ | 1 | d | d | d |
| $C\overline{D}$ | 0 | d | d | d |

$Jb = CD$ ✓

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | d | 0 | d | d |
| $\overline{C}D$ | d | 0 | d | d |
| $CD$ | d | 1 | d | d |
| $C\overline{D}$ | d | 0 | d | d |

$Kb = CD$ ✓

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | 0 | 0 | d | 0 |
| $\overline{C}D$ | 1 | 1 | d | 0 |
| $CD$ | d | d | d | d |
| $C\overline{D}$ | d | d | d | d |

$Jc = \overline{A}D$ ✓

| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | d | d | d | d |
| $\overline{C}D$ | d | d | d | d |
| $CD$ | d | 1 | d | d |
| $C\overline{D}$ | 0 | 0 | d | d |

$Kc = D$ ✓

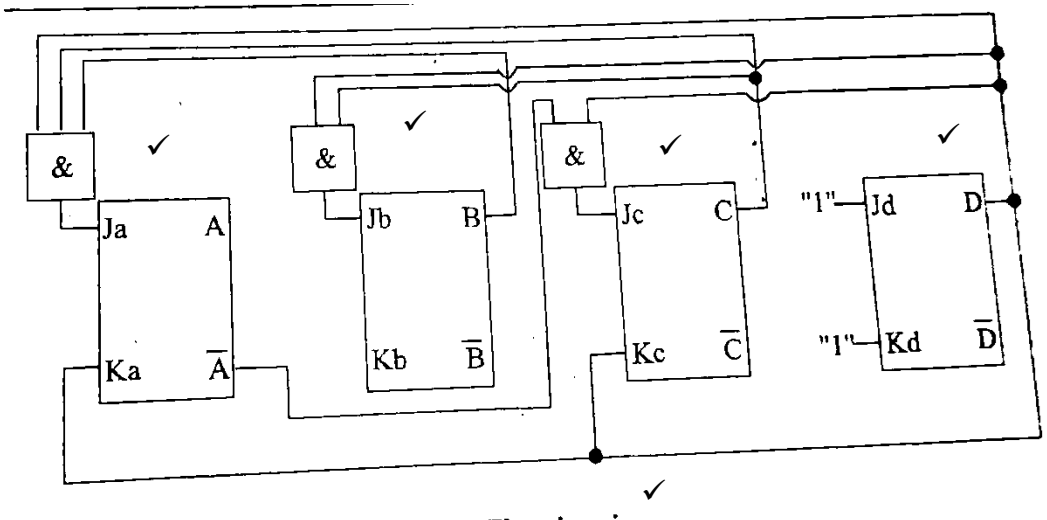
| | $\overline{A}\overline{B}$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | 1 | 1 | d | 1 |
| $\overline{C}D$ | d | d | d | d |
| $CD$ | d | d | d | d |
| $C\overline{D}$ | 1 | 1 | d | d |

$Jd = 1$ ✓

| | $AB$ | $\overline{A}B$ | $AB$ | $A\overline{B}$ |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ | d | d | d | d |
| $\overline{C}D$ | 1 | 1 | d | 1 |
| $CD$ | 1 | 1 | d | d |
| $C\overline{D}$ | d | d | d | d |

$Kd = 1$ ✓

(8)



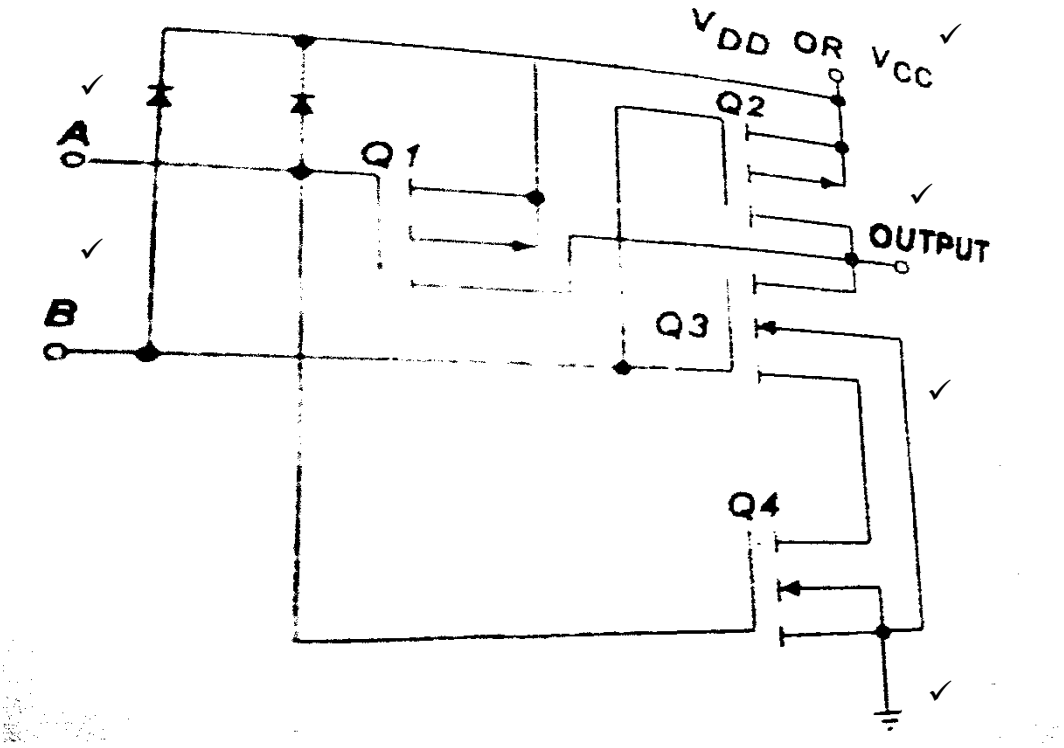

✓

The circuit

(5)
**[23]**

## QUESTION 3

3.1




(6)

3.2 3.2.1 T3/T4.✓✓ (very low output impedance) prevents excessive loading when other TTL gates are connected.✓✓ (4)

3.2.2 T5/T3 and T2/T4.✓✓ (very good current amplifier) because their DC biasing levels are related to one another.✓✓ (4)

3.3

| | TTL | CMOS |
|---|---|---|
| speed | slower | Faster ✓ |
| Packing density | low | High ✓ |
| Power | high | Low ✓ |

(3)
**[17]**

## QUESTION 4

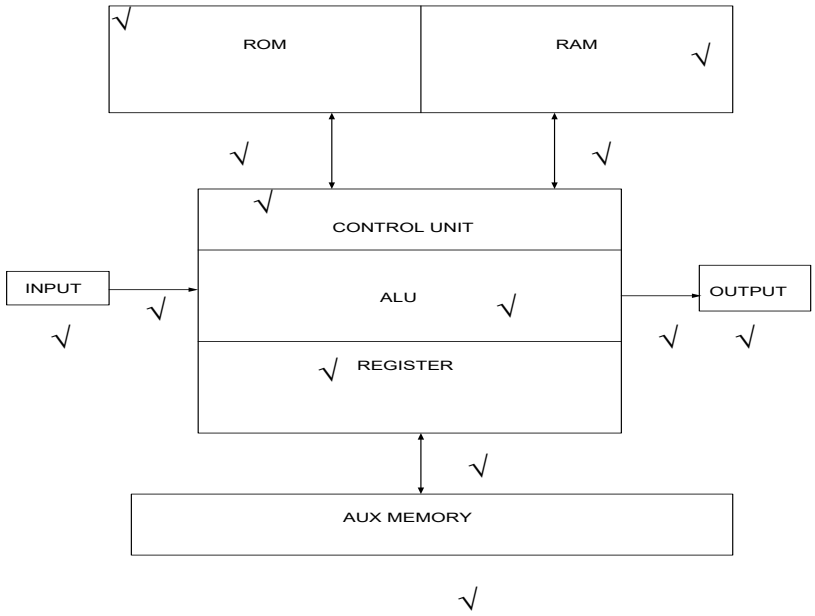
4.1 D
4.2 A
4.3 D
4.4 A
4.5 B
4.6 D
4.7 B
4.8 D
4.9 A
4.10 B

(10 × 1) **[10]**

## QUESTION 5

5.1
- Volatile – loses all information when power is turned off.
- Non-volatile memory – retains information even when power is removed. (2)

5.2



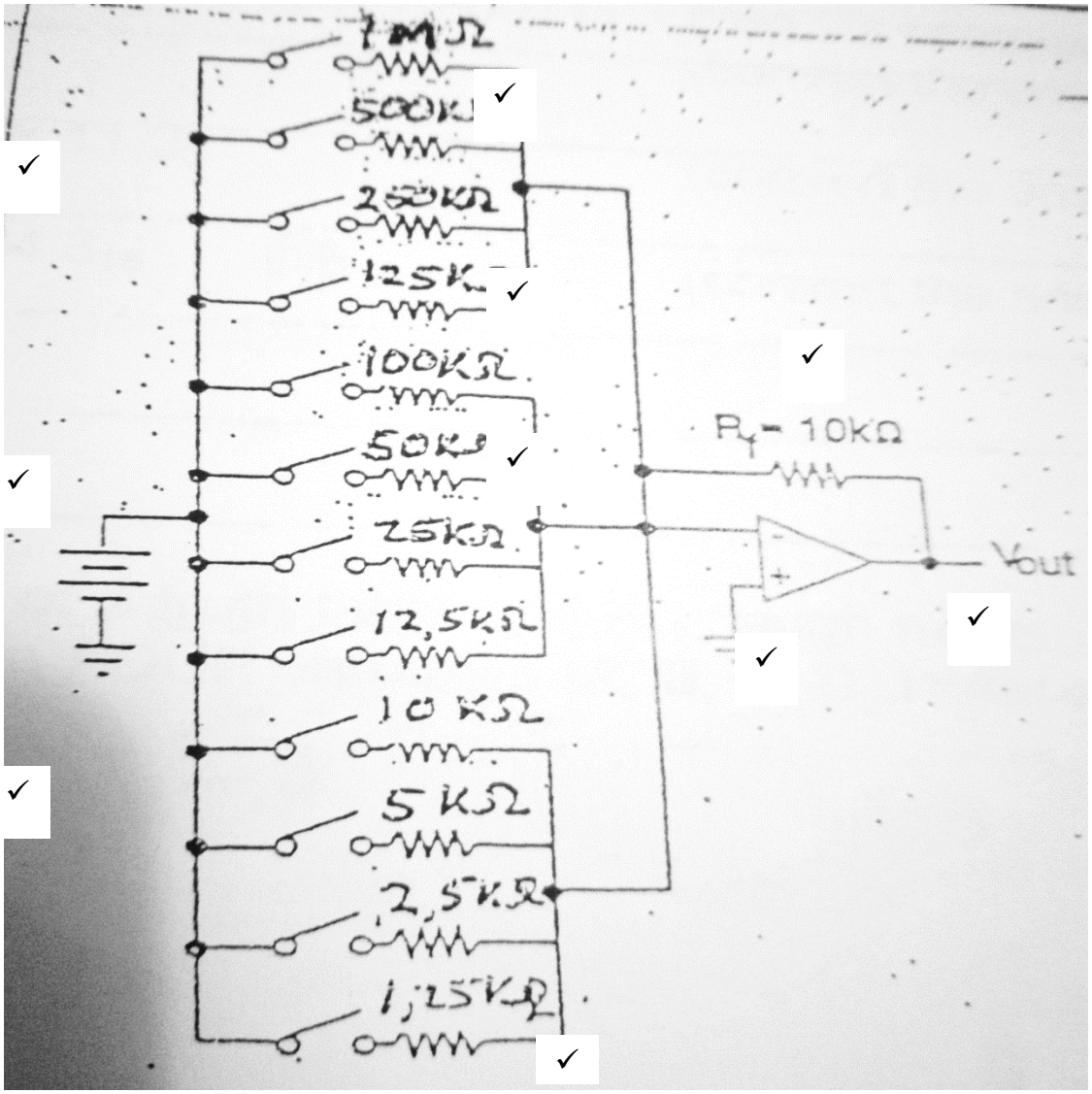

(13)
**[15]**

## QUESTION 6

6.1 Modulator✓/Demodulator✓ – takes high frequency data and changes it into an audio frequency to send over the telephone wires✓ (transmit side-modulation) and takes audio frequencies from the telephone wires and changes them to high frequency data signals✓ (receive side-demodulation). (4)

6.2 To send computer data serially thereby reducing the number of transmission wires needed.✓ It is comprised of a parallel in series-out shift register on the transmit side and a series-in parallel-out shift register on the receive side.✓ It works in the asynchronous mode.✓ (3)
**[7]**

**QUESTION 7**




**[10]**

**TOTAL: 100**

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