higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N5

6 APRIL 2018

This marking guideline consists of 7 pages.

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QUESTION 1

1.1 $135,5_8 = 001\ 011\ 101,101_2 = 1011\ 101,101$ ✓

$21,A_{16} = 0010\ 0001,1010_2$ ✓ $= 1000,101$

$$\begin{array}{r} 10,110 \\ 100001101\overline{)10111\,01101,000} \\ 1000\,1101 \\ \hline 110100110 \\ 100001101 \\ \hline 100110010 \\ 100001101 \\ \hline \ldots 1001010 \end{array}$$

$1011010,101_2 \div 100001,101_2 = 10,110_2$ rem $1001010 \div 100001101$ ✓

Therefore $10,110_2 = 2,68$ ✓ (6)

1.2 $1110001,1_2 - 10001110,111_2$

$01110001,100 \longrightarrow 01110001,100$

$10001110,111 \longrightarrow 01110001,000 + 1 \longrightarrow 01110001,001$

No carry 11100010,101

Therefore the answer is negative – 11100010,101

11100010,101

Subtract 1 from LSB

Complement – 00011101,010

For hex grouping – 0001 1101, 011

Therefore $111001,1_2 - 10001110,111_2 = -0001\ 1101,\ 0110_2 = -1D,6_{16}$ (6)

1.3 $B,C_{16} \times 11,2_8$

$B,C_{16} = 1011,1100 = 1011,11_2$ [each hex no. is represented by 4 binary bits]

$11,2_8 = 001\ 001,\ 010 = 1001,01_2$ [each octal no. is represented by 3 binary]

$$\begin{array}{rr} & 101111 \\ & 100101 \\ \hline & 101111 \\ & 10111100 \\ + & 10111100000 \\ \hline & 110100,1011 \end{array}$$

Shift comma in 4 places 110100,1011

Therefore $1011,11_2 \times 1001,01_2 = 110100,1011_2$

$= 64 + 32 + 8 + 4 + 0,5 + 0,25 + 0,0625$

$= 108,6875_{10}$ (6)

[18]

QUESTION 2

A	**B**	**C**	**D**		**F**
0	0	0	0		1
0	0	0	1		0
0	0	1	0		1
0	0	1	1		0
0	1	0	0		1
0	1	0	1		1
0	1	1	0		1
0	1	1	1		1
1	0	0	0		1
1	0	0	1		0
1	0	1	0		1
1	0	1	1		0
1	1	0	0		1
1	1	0	1		0
1	1	1	0		1
1	1	1	1		0

	$\overline{A}\overline{B}$	$\overline{A}B$	AB	$A\overline{B}$
$\overline{C}\overline{D}$	1	1	1	1
$\overline{C}D$		1		
CD		1		
$C\overline{D}$	1	1	1	1

FROM MAP GROUPINGS

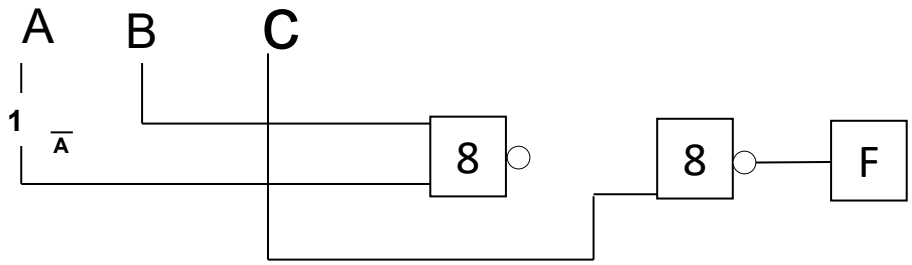
$F = \overline{D} + \overline{A}B$

$= \overline{\overline{\overline{D} + \overline{A}B}}$

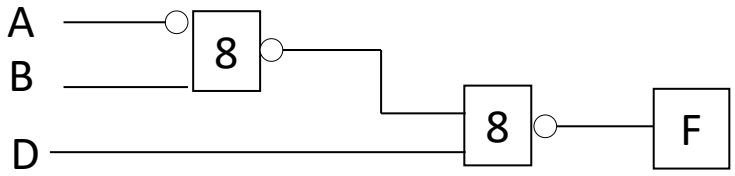
$= \overline{D}.\overline{\overline{A}B}$

$= \overline{D.\overline{\overline{A}B}}$

DRAWING



ALTERNATIVE



[18]

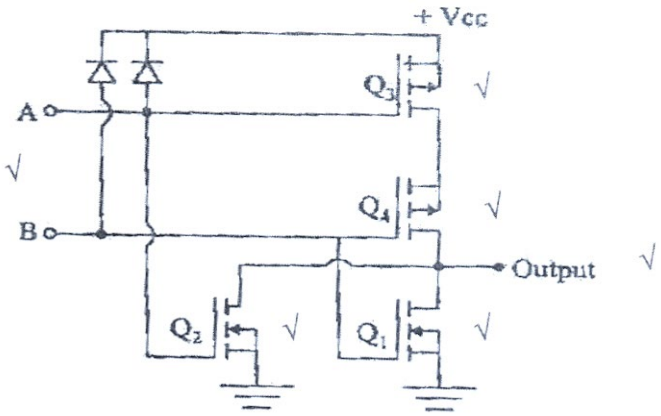
QUESTION 3

3.1 V_{OH} = 30 V; V_{OL} = 0,8 V; V_{IH} = 2,0 V and V_{IL} = 0,4 V

$V_{NH} = V_{OH(MIN)} – V_{IN(MIN)} = 30 – 2 = 28$ V

$V_{NL} = V_{IN(MAX)} – V_{OL(MAXI)} = 0,8 – 0,4 = 0,4$ V (2)

3.2



(6)

3.3 3.3.1 SSI – Small-scale integration
3.3.2 LSI – Large-scale integration
3.3.3 VLSI – Very large-scale integration
3.3.4 ULSI – Ultra-large-scale integration
3.3.5 MSI – Medium-scale integration

(5 × 1) (5)

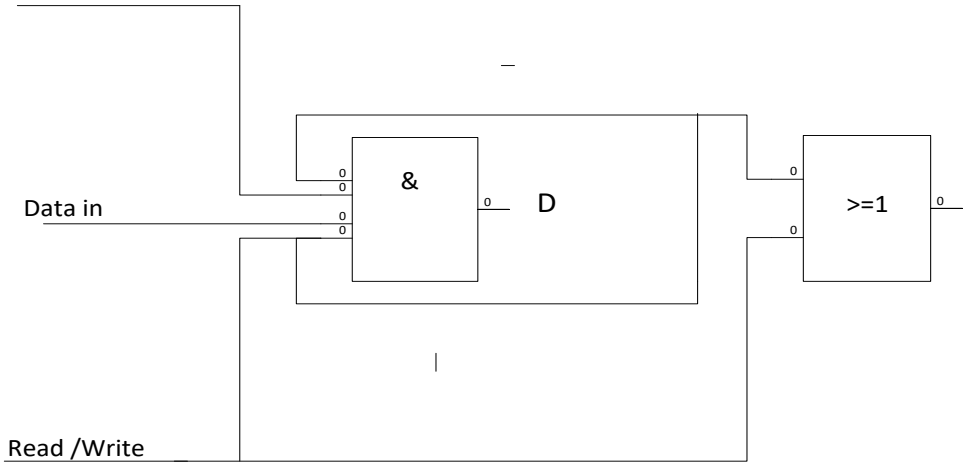
3.4

	SPEED✓	POWER USAGE✓	PACKING DENSITY✓
TTL	Fast	High	Low
CMOS	Slow	Low	High

(3 × 1) (3)
[16]

QUESTION 4

4.1



(6)

4.2
- The ALU (arithmetic logic unit)
- The control unit
- The memory unit
- The input unit
- The output unit (5)

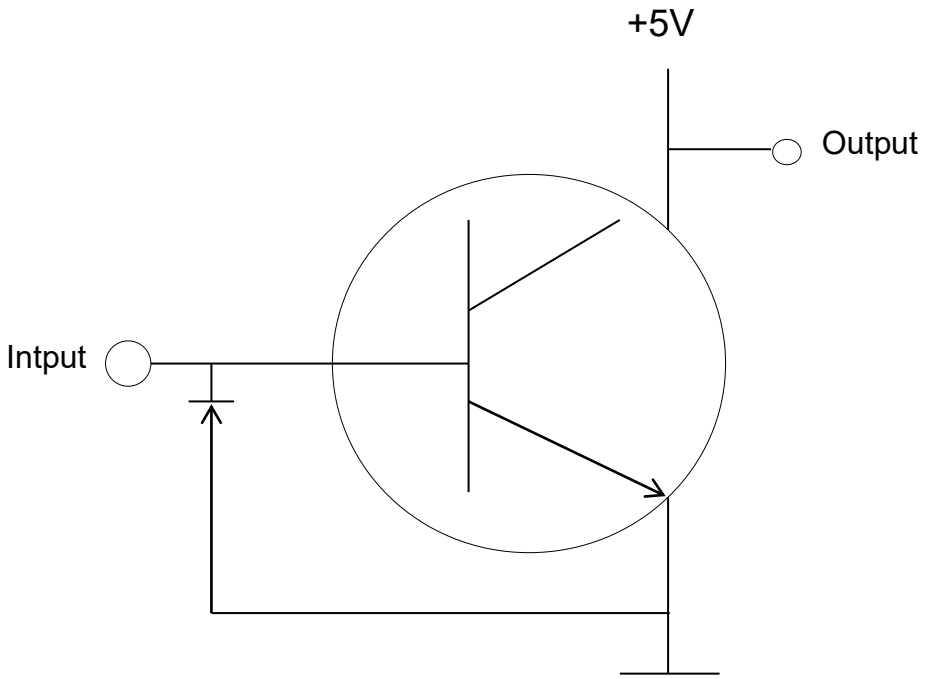
4.3
- The data bus is bi-directional; it carries information between the CPU, micro processor memories and other units/pheripheral devices.
- The address bus is unidirectional; it carries the address code which is used to select data and units from the CPU/micro processor to the pheripheral devices.
- The control bus is bi-directional and carries instruction codes between the CPU/micro processor and other units/pheripheral devices. (6)

[17]

QUESTION 5

5.1
- Silent operation
- Reliability
- Low cost (3)

5.2



(4)

5.3 5.3.1 15 metres

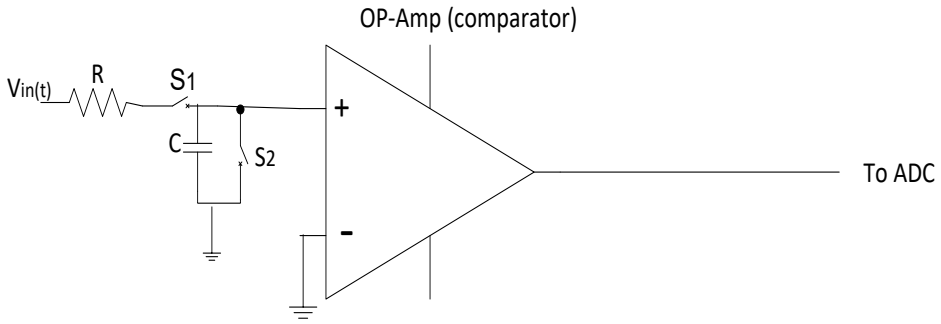
5.3.2 20 000 bits/second

(2 × 1) (2)
[9]

QUESTION 6

6.1 $Vo = \frac{A \times Vin \times time}{RC} = \frac{2424 \times 1 \times 10^{-3}}{100 \times 10^{3} \times 100 \times 10^{-6}} = 0{,}4848\ V$ (2)

6.2



(5)

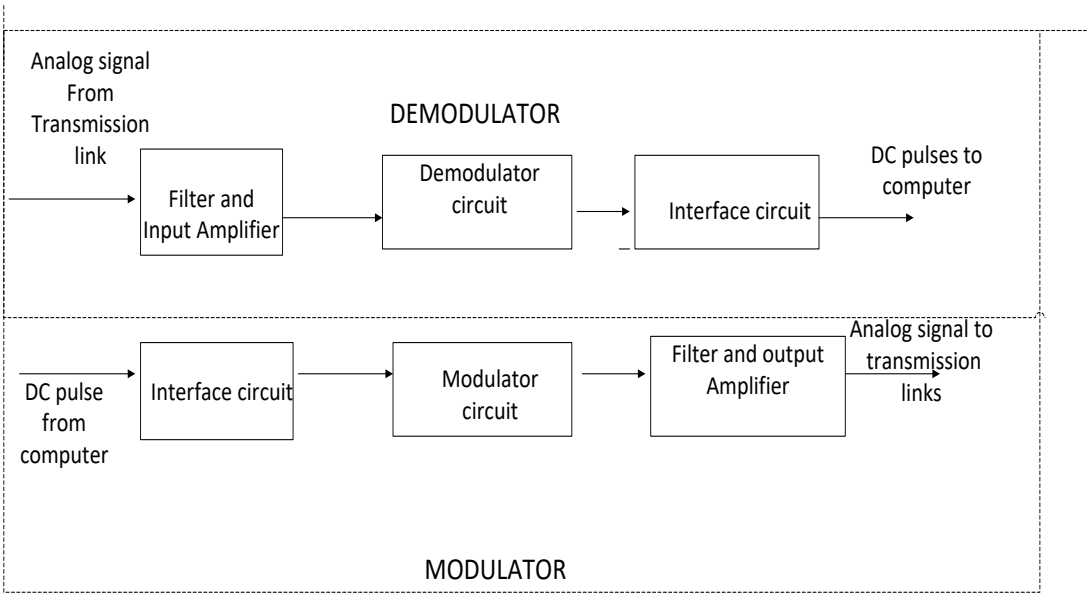
6.3 6.3.1 Linearity – a linear error is a deviation from the ideal output of a DAC.

6.3.2 Threshold – this is the minimum and maximum voltage levels which determine a logic state.

(2 × 2) (4)
[11]

QUESTION 7

7.1



(10)

7.2 To connect digital devices across the telephone wires. (1)
[11]

TOTAL: 100

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