higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N4

XX August 2021

This marking guideline consists of 7 pages.

Copyright reserved

SECTION A

QUESTION 1

1.1 C
1.2 A
1.3 B
1.4 A
1.5 A

(5 × 2) **[10]**

QUESTION 2

2.1 True
2.2 True
2.3 True
2.4 False
2.5 False
2.6 False
2.7 True
2.8 False

(8 × 1) **[8]**

QUESTION 3

3.1 B
3.2 E
3.3 C
3.4 A
3.5 F
3.6 G
3.7 D

(7 × 1) **[7]**

TOTAL SECTION A: 25

SECTION B

QUESTION 4

4.1

BINARY	1'S COMPLEMENT
0 * 0 1 0 0 1 , 0 1 0 0	0 * 0 1 0 0 1 , 0 1 0 0
1 * 0 0 0 1 0 , 0 1 0 1	1 * 1 1 1 0 1 , 1 0 1 0
	1 0 * 0 0 1 1 0 , 1 1 1 0
	1
	0 * 0 0 1 1 0 , 1 1 1 1
	pos 1 1 0 , 1 1 1 1 $_2$

Award ONE mark for each of the following steps indicated correctly:

0 * 0 1 0 0 1 , 0 1 0 ✓

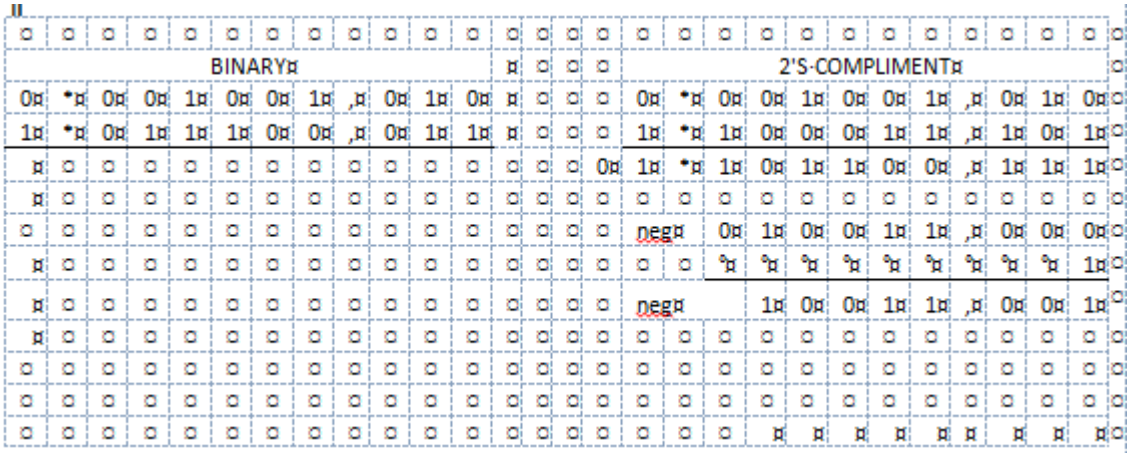
1 * 1 1 1 0 1 , 1 0 1 0 ✓

1 0 * 0 0 1 1 0 , 1 1 1 0 ✓

0 * 0 0 1 1 0 , 1 1 1 1 ✓

pos 1 1 0 , 1 1 1 1 $_2$ ✓ (5)

4.2



Award ONE mark for each of the following steps indicated correctly:

0 * 0 0 1 0 0 1 , 0 1 0 ✓

1 * 1 0 0 0 1 1 , 1 0 1 ✓

0 1 * 1 0 1 1 0 0 , 1 1 1 ✓

negative 0 1 0 0 1 1 , 0 0 0 ✓

negative 0 1 0 0 1 1 , 0 0 1 ✓ (5)

4.3

$$
\begin{array}{rcccccccccc}
 & & & 1 & 0 & 0 & 1 & 0, & 0 & 1 & _2 \\
\text{mult} & & & & & & 1 & 0 & 1 & 1, & 1 \ _2 \\
\hline
 & & & 1 & 0 & 0 & 1 & 0 & 0 & 1 & \\
 & & 1 & 0 & 0 & 1 & 0 & 0 & 1 & & \\
 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & & & \\
1 & 0 & 0 & 1 & 0 & 0 & 1 & & & & \\
\hline
1 & 1 & 0 & 1 & 0 & 0 & 0 & 1, & 1 & 1 & 1 \ _2
\end{array}
$$

Award TWO marks where it was indicated the following number must be added.

$$
\begin{array}{rcccccccc}
 & & 1 & 0 & 0 & 1 & 0 & 0 & 1 & \\
 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & & \\
1 & 0 & 0 & 1 & 0 & 0 & 1 & & & \checkmark \\
\hline
1 & 0 & 0 & 1 & 0 & 0 & 1 & & & \checkmark
\end{array}
$$

Award TWO marks if the answer is correct.

$$1\ 1\ 0\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ _2 \quad \checkmark\checkmark$$

Award ONE mark if the comma is placed in the correct position.

$$1\ 1\ 0\ 1\ 0\ 0\ 0\ 1,\ 1\ 1\ 1\ _2 \quad \checkmark$$ (5)

4.4

$$
\begin{array}{rcccccccccc}
 & & & & & & & & 1 & 0 & 0, \\
\hline
1 & 0 & 0, & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0, \ 0 \ 1 \\
 & & & & & & & 1 & 0 & 0 & 0 \ 0 \ 0 \ 1 \\
\hline
 & & & & & & & & & & 0
\end{array}
$$

Award ONE mark if it was indicated the following value must be deducted:

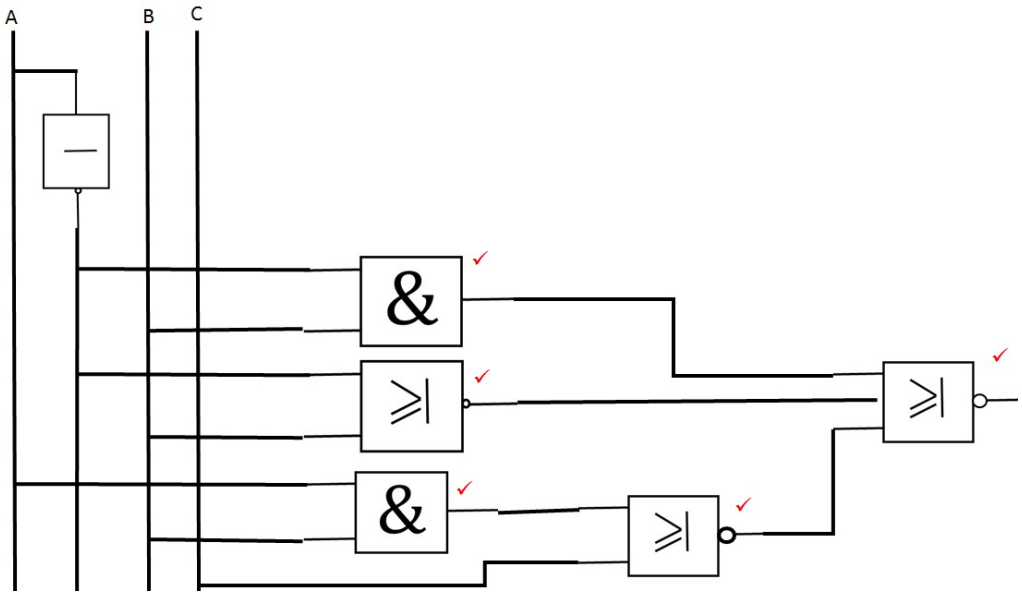
$$1\ 0\ 0\ 0\ 0\ 0\ 1$$

Award ONE mark if it was indicated 0 is left.
Award ONE mark if it was indicated that the answer is 1.
Award ONE mark if the 1 was placed in the correct position.
Award ONE mark if the two 0s was indicated next to the 1.

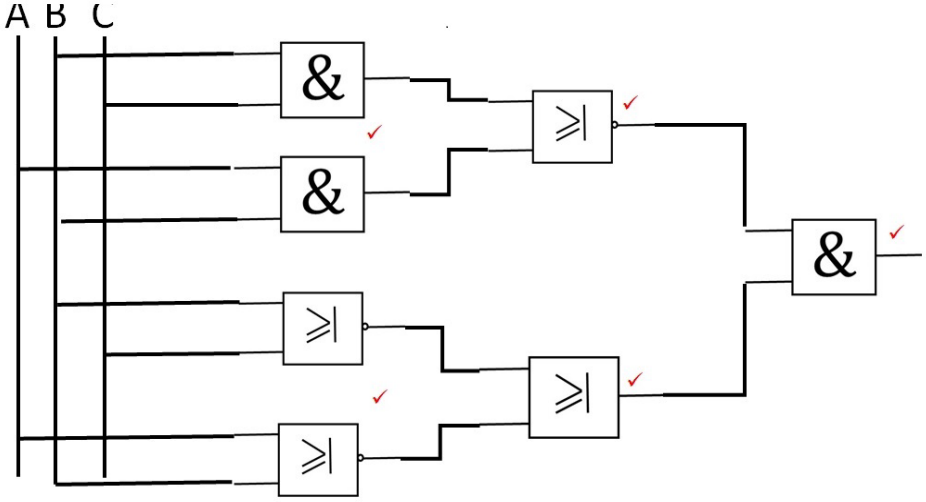
(5)
[20]

QUESTION 5

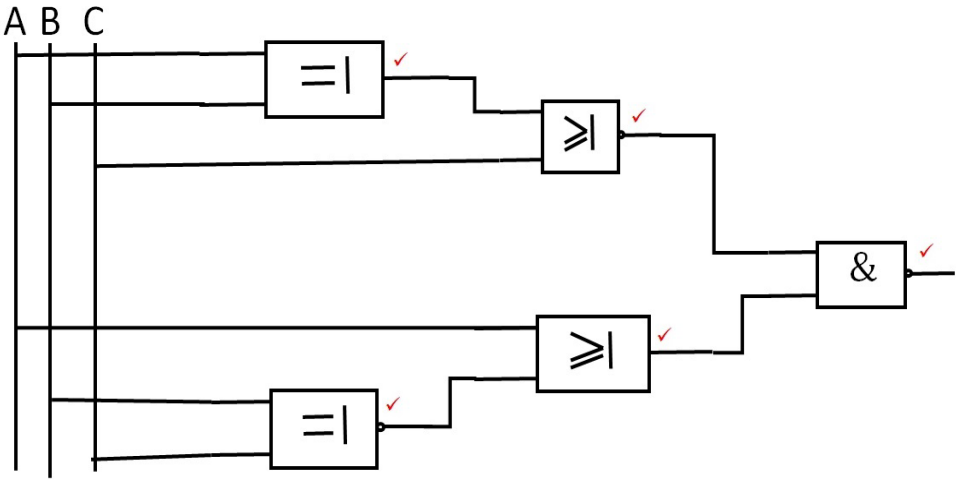
5.1



5.2



5.3



(3 × 5) **[15]**

QUESTION 6

6.1 $\overline{A}BC + A\overline{B}C + \overline{A}B\overline{C} + \overline{A}C\overline{B}$

$= \overline{A}B(C + \overline{C}) + \overline{B}C(A + \overline{A})$ ✓✓

$= \overline{A}B(1) + \overline{B}C(1)$ ✓✓

$= \overline{A}B + \overline{B}C$ ✓

6.2 $C(\overline{A} + \overline{B}) + \overline{A}(B + \overline{C}) + \overline{A}B$

$= \overline{A}(C + \overline{C}) + \overline{B}C + \overline{A}B$ ✓✓

$= \overline{A}(1) + \overline{B}C + \overline{A}B$ ✓

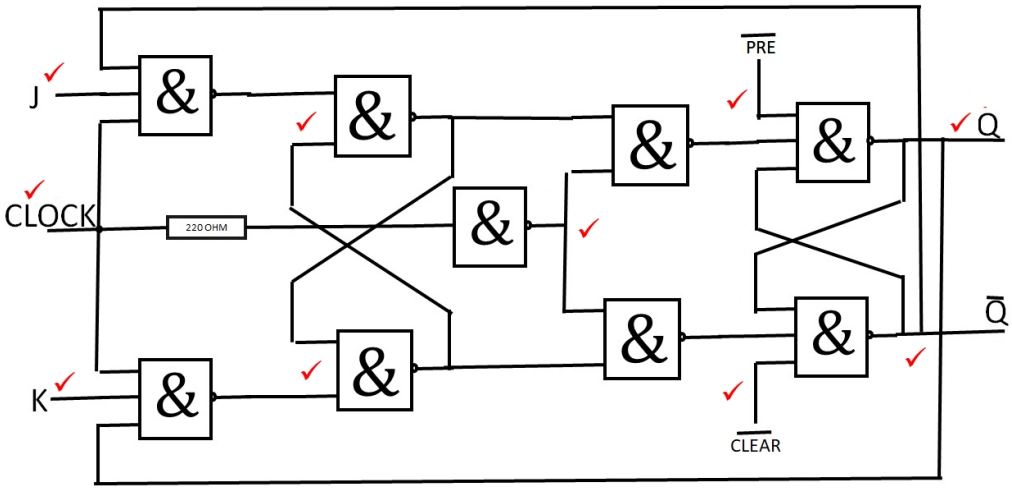
$= \overline{A} + \overline{B}C + \overline{A}B$ ✓

$= \overline{A} + \overline{B}C$ ✓

(2 × 5) **[10]**

QUESTION 7

7.1



Award ONE mark if J is connected correctly.
Award ONE mark if K is connected correctly.
Award ONE mark if the clock is connected correctly.
Award ONE mark if Q is connected correctly.
Award ONE mark if $\overline{Q}$ is connected correctly.
Award TWO marks if the NAND gates in the master are connected correctly.
Award TWO marks if the NAND gates in the slave are connected correctly.
Award ONE mark if the NAND gate between the clock for the master and the slave is connected correctly. (10)

7.2 If the set or the pre-set line is activated by changing it to a 0, Q will become a 1 and $\overline{Q}$ will become a 0.✓✓

If the reset or the clear line is activated by changing it to a 0, $\overline{Q}$ will become a 1 and Q will become a 0.✓✓ (4)

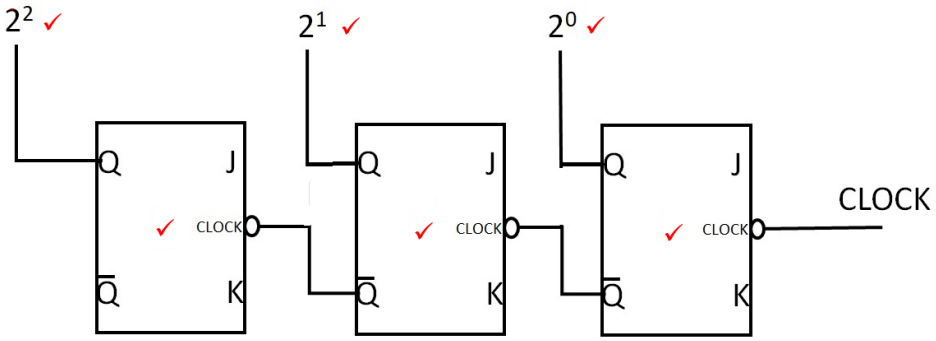
7.3 When the clock on the master is a 1, the clock on the slave will be a 0.✓

When the clock on the master is a 0, the clock on the slave will be a 1.✓

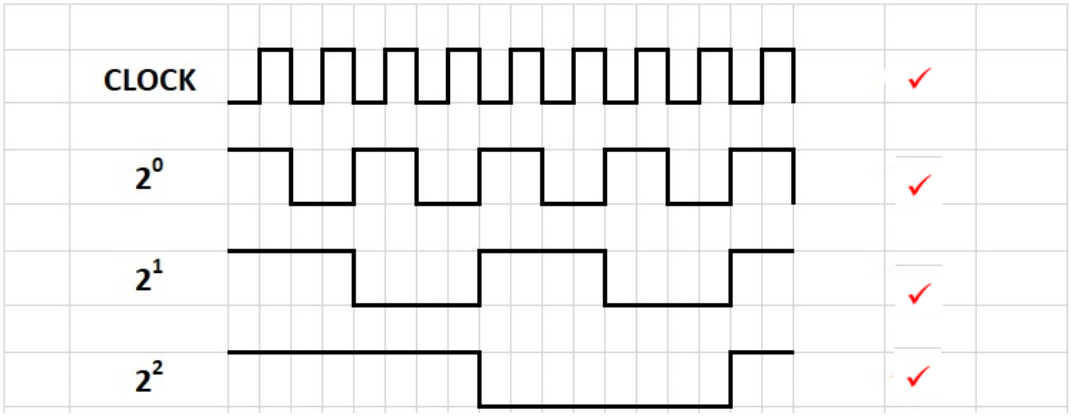
To be able to change Q and $\overline{Q}$, the clock on the slave must change from a 0 to a 1.✓✓

Therefore, the clock on the master will have to change from a 1 to a 0 for the clock on the slave to change from a 0 to a 1.✓✓ (6)

7.4 (10)



Any other applicable counter will be acceptable.



[30]

TOTAL SECTION B: 75
GRAND TOTAL: 100

Copyright reserved