higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N4

(8080354)

19 April 2021 (X-paper)
09:00–12:00

Nonprogrammable calculators and drawing instruments may be used.

This question paper consists of 7 pages.

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
DIGITAL ELECTRONICS N4
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer all the questions.
2. Read all the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Diagrams should be large and neat and may be done in pencil.
5. Use only a black or blue pen.
6. Write neatly and legibly.

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QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 A/An … is a logic gate with an output of binary 1, if one input is at binary 1 and the other input at binary 0.

A NOT gate
B AND gate
C exclusive-OR gate
D NOR gate

1.1.2 A/An … is a logic gate with one input and one output.

A NOR gate
B AND gate
C NOT gate
D NAND gate

1.1.3 A logic gate comprising of an OR function plus a NOT function, is a/an ...

A exclusive-OR gate.
B NOT gate.
C NAND gate.
D NOR gate.

1.1.4 The equality comparator is a/an …

A exclusive-OR gate.
B AND gate.
C exclusive-NOR gate.
D NOR gate.

1.1.5 The logic gate with an output which is always the inverse of its input is a/an …

A OR gate.
B NOT gate.
C NAND gate.
D NOR gate.

(5 × 1) (5)

1.2 Complete the following sentences by writing only the missing word next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

1.2.1 The exclusive-NOR gate is also known as the … comparator.

1.2.2 The NAND gate is a combination of the AND gate and the … gate.

1.2.3 … parity checks are designed to detect a double-digital error.

1.2.4 The … code is a single error detecting code.

1.2.5 The hexadecimal system has a … of 16.

(5 × 1) (5)

1.3 Choose an item from COLUMN B that matches a description in COLUMN A. Write only the letter (A–E) next to the question number (1.3.1–1.3.5) in the ANSWER BOOK.

COLUMN A		COLUMN B	
1.3.1	The voltage difference between the logic levels of 1 and 0	A	loading
1.3.2	The maximum number of standard inputs that can reliably be driven by one output	B	logic swing
1.3.3	The output of one flip-flop serves as the clock pulse of the next flip-flop	C	threshold voltage
1.3.4	Circulating shift register	D	asynchronous clocking
1.3.5	The minimum and maximum voltage levels which determine the logic state	E	ring counter

(5 × 1) (5)

1.4 Indicate whether the following statements are TRUE or FALSE by writing only 'True' or 'False' next to the question number (1.4.1–1.4.5) in the ANSWER BOOK.

1.4.1 An astable multivibrator is a free-running clock-pulse generator which oscillates only when the enable line is held at logic 0.

1.4.2 Shift registers are used to transfer the information from one register to the next register one bit at a time.

1.4.3 Counters make use of flip-flops based on the toggle action.

1.4.4 Small-scale integration refers to ICs of which the complexity is comparable to logic circuits with 100 gates or more.

1.4.5 The pulse repetition frequency of a square wave pulse train is the number of pulses generated in one second.

(5 × 1) (5)

1.5 Choose ONE term from the list below for each of the following descriptions and write it next to the question number (1.5.1–1.5.5) in the ANSWER BOOK.

bandwidth; alphanumeric; code; demultiplexing; set

1.5.1 An input that forces the Q output of a memory element to one (‘1’)

1.5.2 A process which is used to send a single signal through multiple channels

1.5.3 The range of frequencies occupied by a modulated radio-frequency signal, usually given in hertz

1.5.4 Code that can recognise numbers, letters and devised characters

1.5.5 Numbers, letters or words represented by a specific group of symbols

(5 × 1) (5)

1.6 Choose the correct term from those given in brackets. Write only the answer next to the question number (1.6.1–1.6.5) in the ANSWER BOOK.

1.6.1 For an (up-counter/down counter) the Q output is connected to the clock-pulse input of the next flip-flop.

1.6.2 The SR latch using (NAND/NOR) gates switches on a negative-going pulse.

1.6.3 In a (D-type/T-type) JK master/slave flip-flop the output is fed back to the input.

1.6.4 The Gray-code is an example of a (weighted/non-weighted) code.

1.6.5 In the (even/odd) parity system the parity bit is used to ensure that the total number of 1’s when added together equals an even number.

(5 × 1) (5)

[30]

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QUESTION 2

2.1 Subtract the following by means of the two's complement method and convert the final answer to the decimal system:

2.1.1 $AD,7_{16} - 65,5_8$

2.1.2 $BF,C_{16} - DB,9_{16}$

(2 × 6) (12)

2.2 Calculate the following in their binary form and convert the final answer to the decimal system.

2.2.1 $A9,7_{16} \div 7,5_8$

2.2.2 $E4,3_{16} \times 25,3_8$

(2 × 6) (12)

2.3 Convert $86,5_{10}$ to the following BCD codes:

2.3.1 2421

2.3.2 4221

2.3.3 5211

(3 × 2) (6)

[30]

QUESTION 3

3.1 Simplify the following Boolean expressions:

3.1.1 $\overline{A}\,\overline{B} + A\,\overline{B}\,\overline{D} + D$ (4)

3.1.2 $AB\overline{C}D + ABC\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,\overline{D}$ (6)

3.2 Make a neat, labelled sketch of the logic circuit of the following Boolean expression without simplifying:

$\overline{\overline{(AD + C)}\,AB} + \overline{ABC} = F$ (6)

[16]

QUESTION 4

Make a neat, labelled sketch of each of the following circuit diagrams:

4.1 Serial binary adder (8)

4.2 Module 8 down counter (6)

[14]

QUESTION 5

Make a neat, labelled sketch of each of the following circuit diagrams:

5.1 D-latch flip-flop (5)

5.2 1 line to 4 lines demultiplexer system (5)

[10]

TOTAL: 100

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