higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE (VOCATIONAL)

ELECTRONIC CONTROL AND DIGITAL ELECTRONICS
NQF LEVEL 4

2 March 2020

This marking guideline consists of 7 pages.

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QUESTION 1

1.1. 1.1.1 Ahead
1.1.2 Ohms
1.1.3 Resonance
1.1.4 180
1.1.5 In phase

(1 × 5) (5)

1.2 1.2.1 $C = \frac{1}{2\pi f Xc}$ ✓

$= \frac{1}{2\pi \times 50 \times 27}$ ✓

= 117,89µF✓ (3)

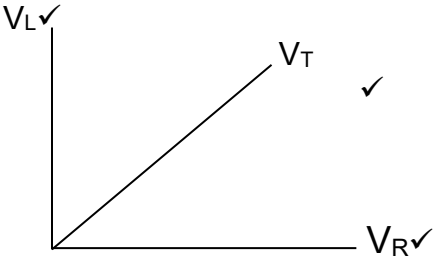
1.2.2 The current flow would increase through the capacitor.✓ If the frequency of the supply is increased, the capacitive reactance will decrease✓ as it is indirectly proportional to the frequency of the supply.✓ (3)

1.3 1.3.1 $Z = \sqrt{R^2 + X_L^2}$
$= \sqrt{60^2 + 90^2}$ ✓
= 108,167Ω✓ (2)

1.3.2 $I_T = V/Z$
= 100/108,167
= 0,924A✓✓ (2)

1.3.3 $V_R = IR$
= 0,924 X 70
= 64,714V✓

$V_L = IX_L$
= 0,924 X 90
= 83.16V✓



(5)
[20]

QUESTION 2

2.1
2.1.1 C
2.1.2 B
2.1.3 D
2.1.4 C
2.1.5 B

(1 × 5) (5)

2.2 $$F_0 = \frac{1}{2\pi RC\sqrt{6}} \checkmark = \frac{1}{2\pi \times 2200 \times 0{,}22 \times 10^{-6}\sqrt{6}} \checkmark = 134{,}245\text{Hz} \checkmark$$ (3)

2.3 2.3.1
- No signal power is lost in the collector or base resistors because of the low winding resistance of the transformer.
- It provides a higher voltage gain than the RC coupled amplifier.
- It provides excellent impedance matching between stages. (3)

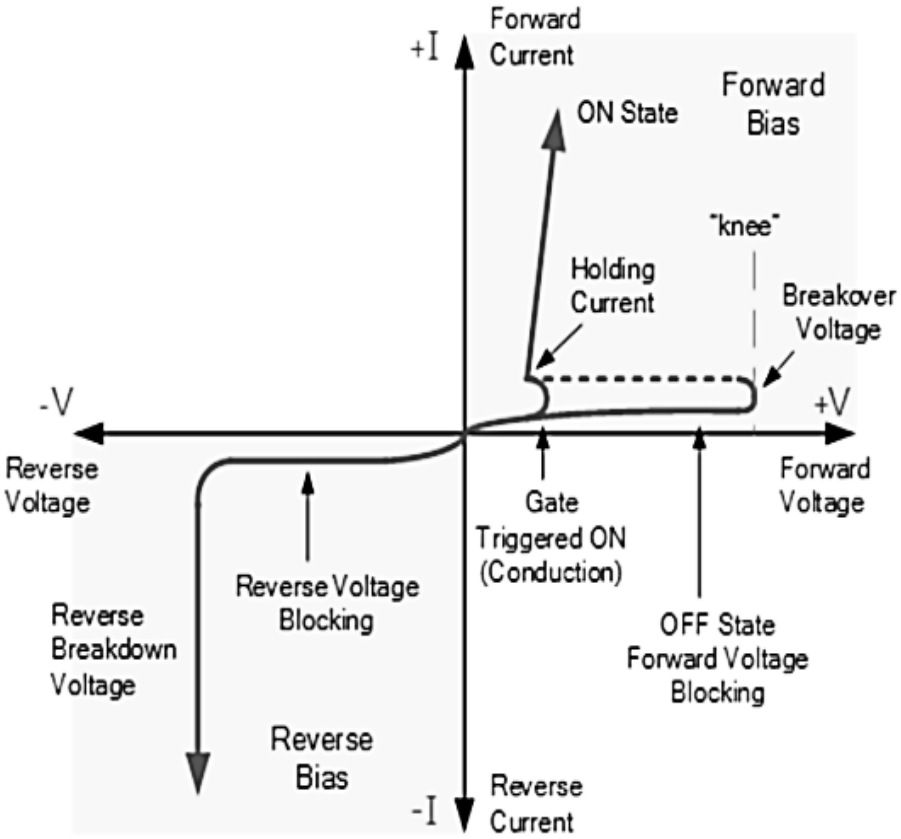
2.3.2
- It is very expensive and bulky, particularly when operated at audio frequencies.
- It produces a hum in the circuit.
- The winding inductance may produce reverse frequency distortion. (3)

2.3.3 It is useful in multistage amplifiers where it is used as a final stage. (1)

2.4
- The output current flows only for one cycle or 180^0 of the input signal.
- The transistor dissipates no power with zero input signals.
- The average current drawn by the circuit is smaller than that of a class A amplifier.
- It has an efficiency of 78%. (4)

2.5
- The operating temperature
- A change in base-emitter voltage V_{BE}
- Transistor current gain (β) (3)

2.6



TWO marks for the correct curve
SIX marks for: Holding current
Off state
On state
Reverse voltage blocking
Reverse Bias side
Forward Bias side (2 + 6) (8)

[30]

QUESTION 3

3.1 3.1.1 $V_{CEO\ (min)}$ = 45✓ , $I_{C(max)}$ = 3✓, P_D = 15✓, h_{FE} = 20✓ and the transistor polarity is NPN✓ (5)

3.1.2 Casing is TO-18✓, polarity is NPN✓, $V_{CE\ (SAT)}$ = 0.6✓, I_C = 100✓, F_T = 300✓ (5)

3.2 3.2.1 BZY97 – basic type of a zener diode (1)

3.2.2 C - ± 5% tolerance (1)

3.2.3 8V2 – 8,2 volts (1)

3.3 3.3.1 D
3.3.2 C
3.3.3 B
3.3.4 F
3.3.5 A
(1 × 5) (5)

3.4
- The strips of copper tracks can get loose after components have been changed several times.
- When a copper tracks breaks, it may leave an invisible hairline of copper.
- The relationship between components and circuit diagrams may be confusing for beginners since the connecting tracks and where they are broken cannot be seen from the component side. (2)

[20]

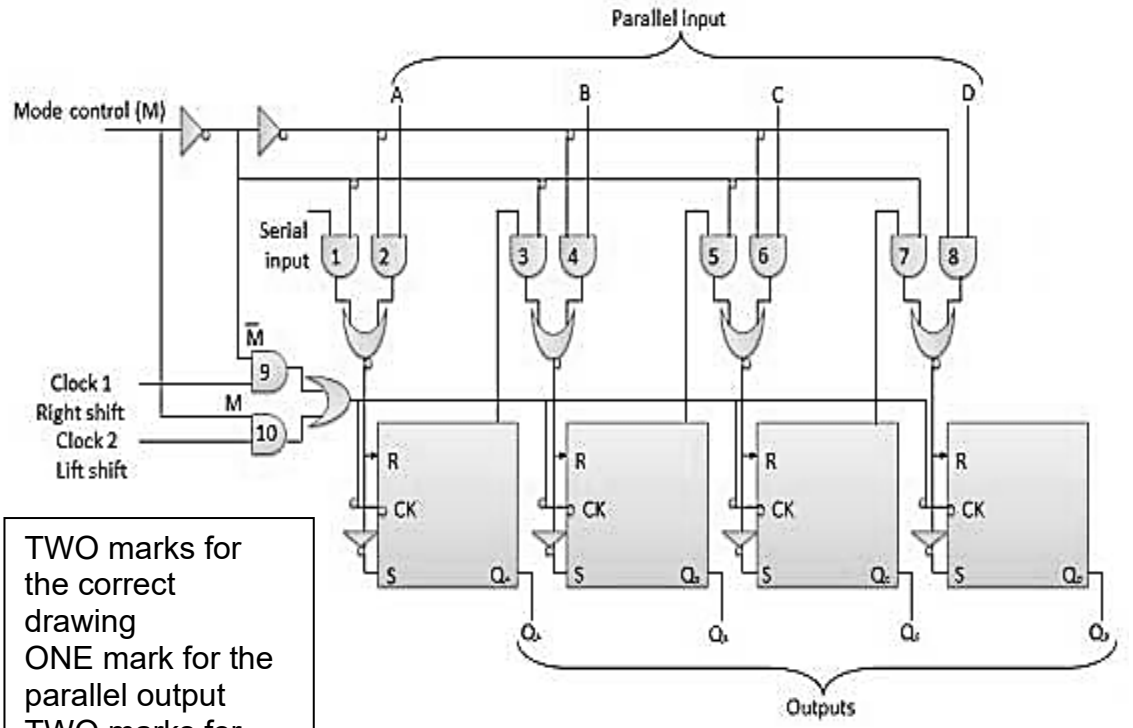
QUESTION 4

4.1

A	B	C	F
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1

ONE mark for ALL correct values of B
ONE mark for ALL correct value of F (2)

4.2



TWO marks for the correct drawing
ONE mark for the parallel output
TWO marks for the left/right control

- The diagram above shows Bi-directional Shift register, this type of register allows shifting of data✓either to the left side or to the right side.✓
- It is implemented by using logic gate circuitry that enables the transfer of data from one stage to the next stage✓ to left or to the right, depending on the level of a control line.✓
- The RIGHT/LEFT is the control input signal which allows data shifting either towards right or towards left.✓A high on this line enables the shifting of data towards right and a low enables it towards left.✓
- When RIGHT/LEFT signal is high,✓ out of the pair of each 2 AND gates the first AND gate from each of the pair is enabled.✓
- The state of the Q output of each Flip Flop is passed through the input of the following flip flop. When the clock pulse arrives, the data are shifted one place to the right.✓
- When *RIGHT*/*LEFT* − − − − − − RIGHT/LEFT_ signal is low,✓out of the pair of each 2 AND gates the second AND gate from each of the pair is enabled.✓
- The state of the Q output of each Flip Flop is passed through the input of the preceding flip flop.✓ When the clock pulse arrives, the data are shifted one place to the left.✓

(13)
[15]

QUESTION 5

5.1 When input X_0 is activated momentarily, output Y_0 becomes energised and will latch itself via normal open contact Y_0, situated below input X_0. ✓At the same time, input Y_0 in rung three was activated momentarily which activated the timer. ✓ The timer started timing out, but X_0 was released before the pre-set time had lapsed and the timer reset itself since its power was removed.✓

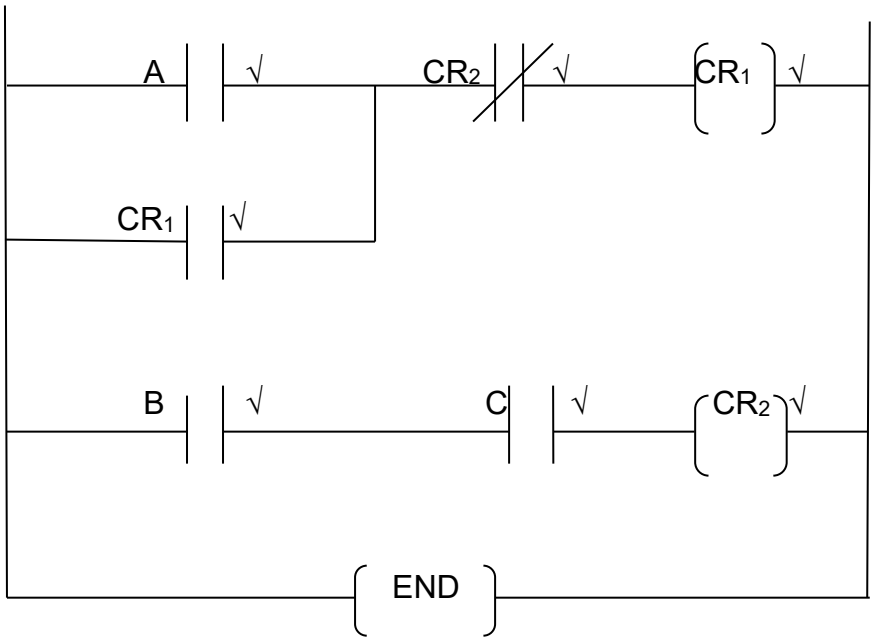
The output coil Y_0 will remain energised and the circuit will remain in this state even if the input X_0 should be activated or held down for a period less than 20 seconds. ✓Should input X_0 be activated for a period exceeding 20 seconds, timer T_0 would count out and produce an output which would change the logic of all other elements having the same address.✓

The NC contact T_0 in rung one will change from logic 1 to 0 de-energising the output coil Y_0 that in turn will de-activate the latch contact Y_0 in rung two.✓

The output coil Y_0 will now be OFF (logic 0) and remain in this state until the input X_0 changes from logic 0 to logic 1.✓

Application: application requiring only one switch to perform both the ON and OFF functions such as irrigation system or intercoms networks.✓ (8)

5.2



(7)
[15]

TOTAL: 100

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