higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N6

18 November 2022

This marking guideline consists of 5 pages.

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QUESTION 1

1.1	1.1.1	G
	1.1.2	A
	1.1.3	H
	1.1.4	B
	1.1.5	I
	1.1.6	K
	1.1.7	E
	1.1.8	F
	1.1.9	M
	1.1.10	T
	1.1.11	N
	1.1.12	O
	1.1.13	Q
	1.1.14	R
	1.1.15	S

(15 × 1) (15)

1.2 1.2.1 True✓– The IR holds the whole instruction word. Op – Code plus Operand address.✓

1.2.2 False✓ – The Program Counter holds the address of the next instruction.✓

1.2.3 False✓ – All operations are synchronised by the system clock. ✓

1.2.4 False✓ – Relay logic is outdated but still used in some PLCs .Cell phones use digital logic signals from Integrated circuits.✓

1.2.5 False✓ – The interface is a port. The bus is internal in the computer.✓

(5 × 2) (10)
[25]

QUESTION 2

2.1 The smallest change that can occur in the analogue output✓ as a result of a change in the digital input✓ of a D/A converter.

2.2 Accuracy determines how close the actual analogue output✓ is to the theoretically expected value of the digital input.✓

2.3 It is the time required to produce a stable analogue output voltage✓ when the digital input changes.✓ It depends upon the word length and type of circuit used.

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2.4 It occurs when the input/output transfer function of a D/A converter is not perfect.✓ A monolithic converter is one where the output increases the same as an increase in input.✓

2.5 The deviation from the minimum output voltage expected✓ when the minimum input code is applied. Example code 0000 should give 0 volt output.✓

(5 × 2) **[10]**

QUESTION 3

3.1 3.1.1 Data bus is used to transfer information✓ (data) in both directions✓ between any two devices. It is bi-directional and has a requirement of tri -state for any peripheral or device✓ that needs connectivity to the bus.

3.1.2 Purpose of the address bus is to select a device✓ which needs to be engaged to enable the transfer of information.✓ More than one device can be connected or addressed by the address bus.
It specifies a specific memory location.✓

3.1.3 The control bus conveys control signals✓ to the rest of the computer. Control signals are responsible for synchronising the operation✓ of the different units within the system and the control unit is part of the CPU.✓

3.1.4 The control unit is part of the CPU✓ together with the ALU. The control unit processes instructions. It interprets an instruction✓ and issues a control signal to the ALU to select which function needs to✓ be performed and when by the ALU and other units.

3.1.5 Any program (high or low level language)✓ need to be ultimately converted into its simplest form✓ which is machine language before it can be executed by the processor. This machine code consists of zero's and one's, and is in binary✓ format.

(5 × 3) (15)

3.2
- Hardware interrupt requests✓ are issued by external devices and peripherals✓ connected to the computer system. They send interrupt✓ signals to the CPU in asynchronous mode.✓ After receiving it and acknowledgement, he processor then executes an interrupt service routine issued by the hardware.✓
- Software interrupts are program driven instructions✓ inserted at desired locations in a program.✓ When a software interrupt instruction✓ is executed in the program, the processor✓ then executes an interrupt service routine.✓

(2 × 5) (10)
[25]

QUESTION 4

4.1 $x = u^2 - ut$

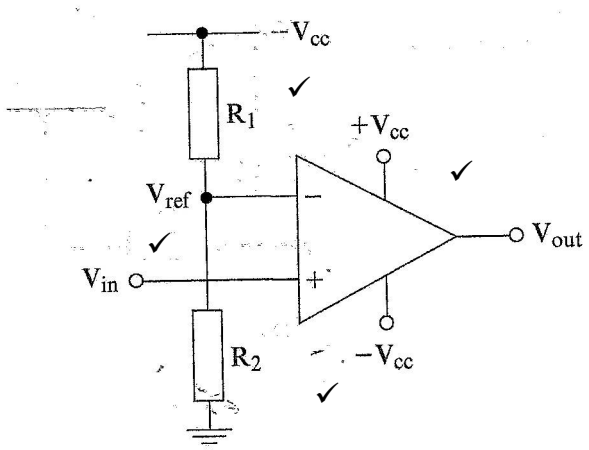
Mathematical operations done before coding:

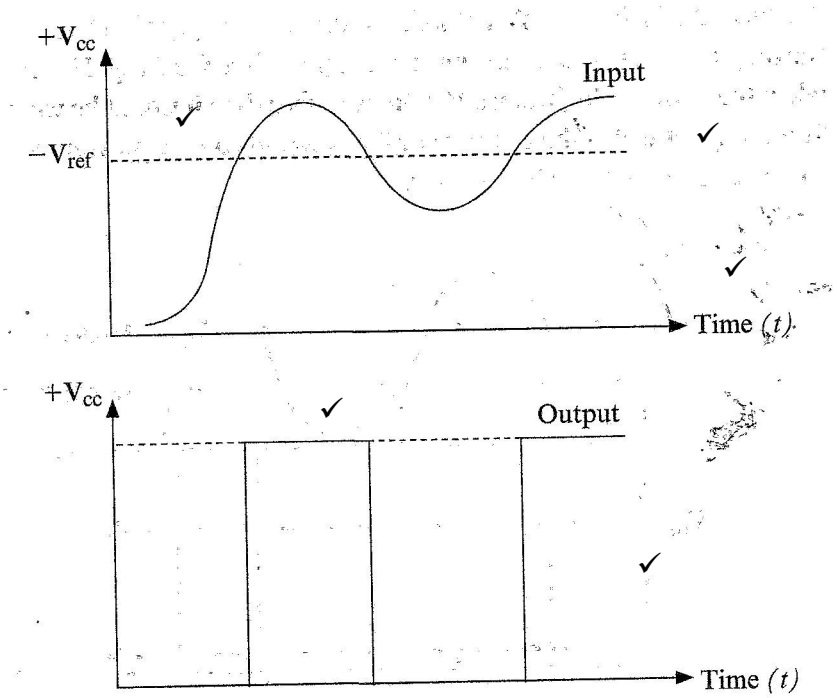
$x = u^2 - ut$
$x = uu - ut$
$x = u(u - t)$✓

INSTRUCTION LOCATION	INSTRUCTION WORD		DESCRIPTION
	OP-CODE	ADDRESS	
CCAA	LOAD	F1B4	Load u ✓
CCAB	SUBT	F1B3	Subtract t✓
CCAC	BRAP	CCB1	Branch if Acc > 0✓
CCAD	MULT	F1B4	Multiply by u✓
CCAE	BRAP	CCB1	Branch if Acc > 0✓
CCAF	STOR	F1B7	Store in x ✓
CCB0✓	OUTP		Output ✓
CCB1	HALT		Halt ✓

Note that other programming sequences are also accepted. (10)

4.2

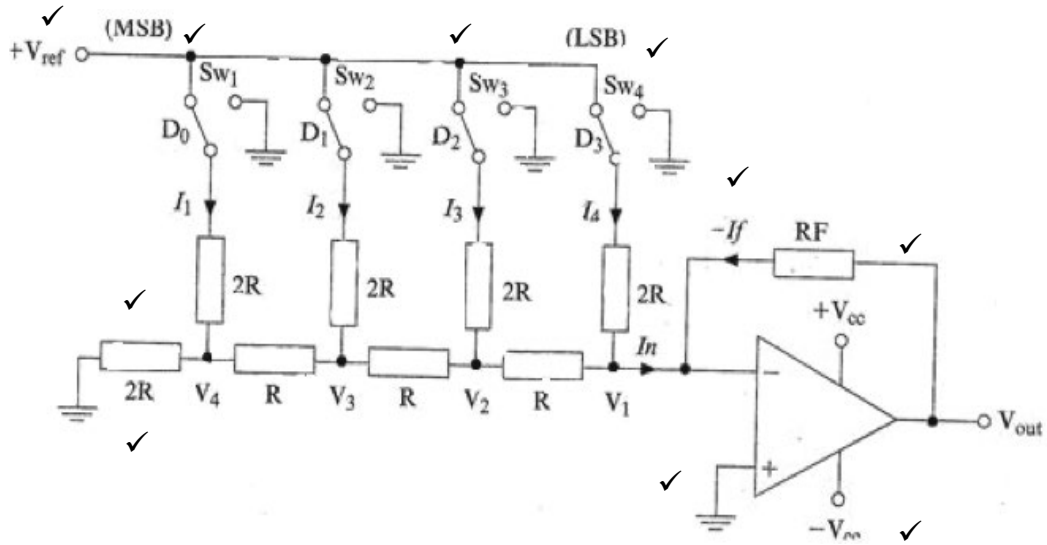




(10)
[20]

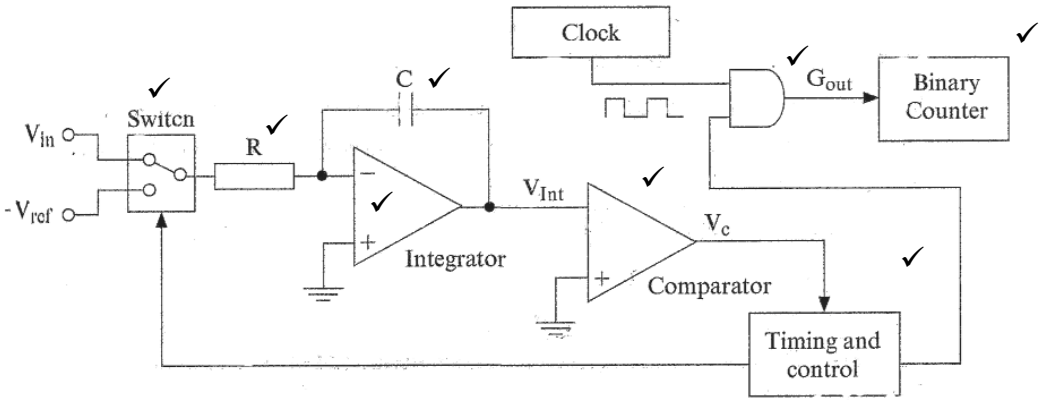
QUESTION 5

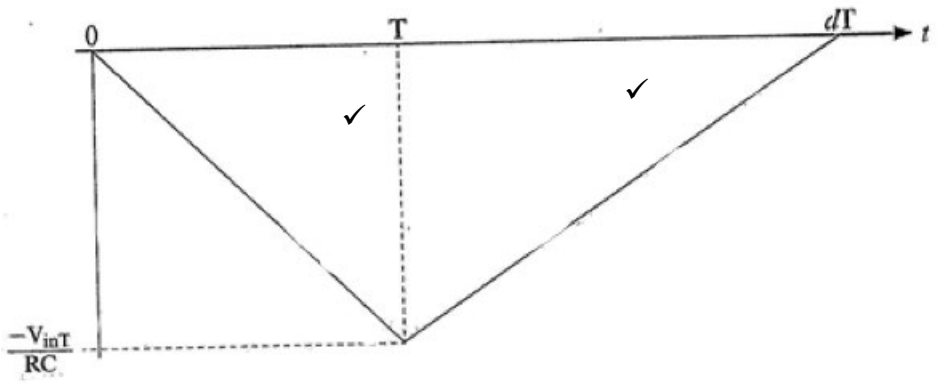
5.1



(10)

5.2





(10)
[20]

TOTAL 100

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