higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N6

24 NOVEMBER 2023

This marking guideline consists of 7 pages.

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QUESTION 1

1.1 False
If there is no JUMP instruction, the program counter will INCREMENT: PC + 1.

1.2 False
The instruction register holds OP CODE as well.

1.3 False
The program counter holds the address of the next instruction to be carried out.

1.4 True
Data stored on magnetic tape is accessed (read or write) serially in a sequential order.

1.5 False
The Microsoft Office suite is not open-source software. You do not buy the source code when you buy Microsoft Office. Microsoft owns the source code and they do not allow end users to alter it.

1.6 False
The DMA controller takes over control of the processor and transfers data to and from the memory over the system bus.

1.7 True
The control unit and access to memory and all CPU operations are synchronised to the system clock oscillator.

1.8 False
Both machine code and assembler are low-level languages and are non-portable.

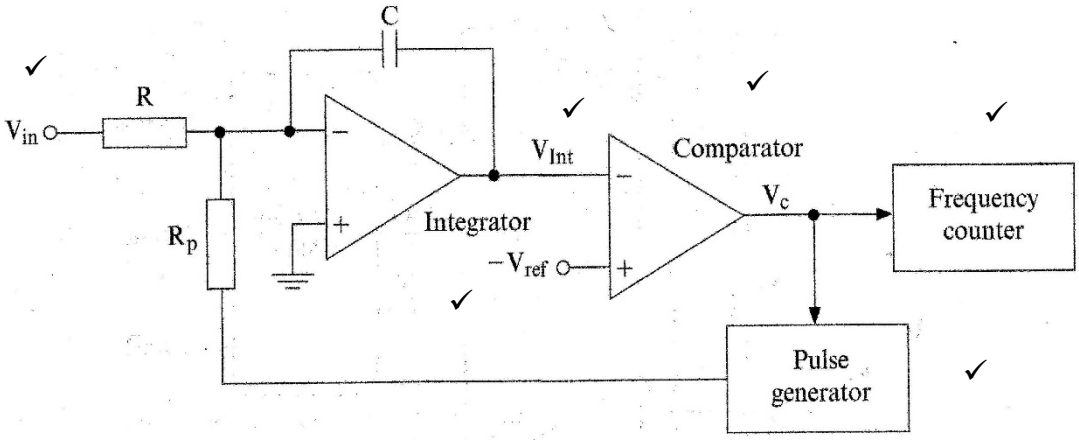
1.9 False
READ reads from the RAM memory.

1.10 True
The accumulator stores the ongoing computational outputs from the ALU.

(10 × 2) **[20]**

QUESTION 2

2.1 Voltage-to-frequency-to-digital converter

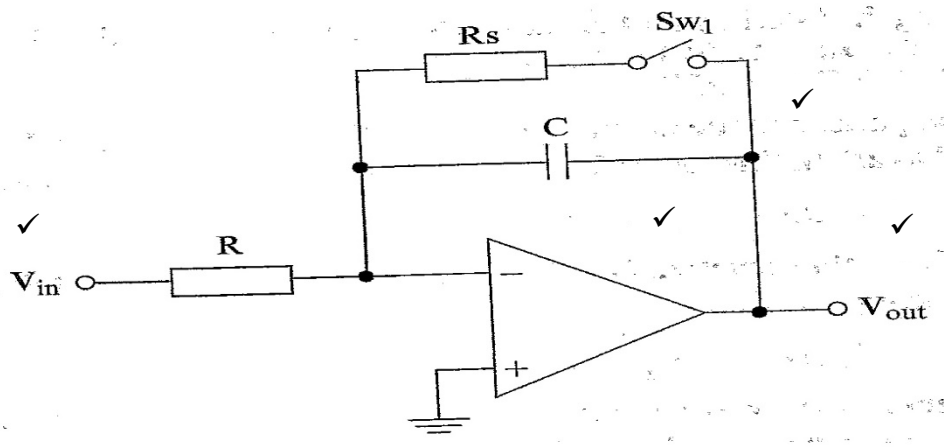


(6)

2.2 Operation of voltage-to-frequency-to-digital converter:

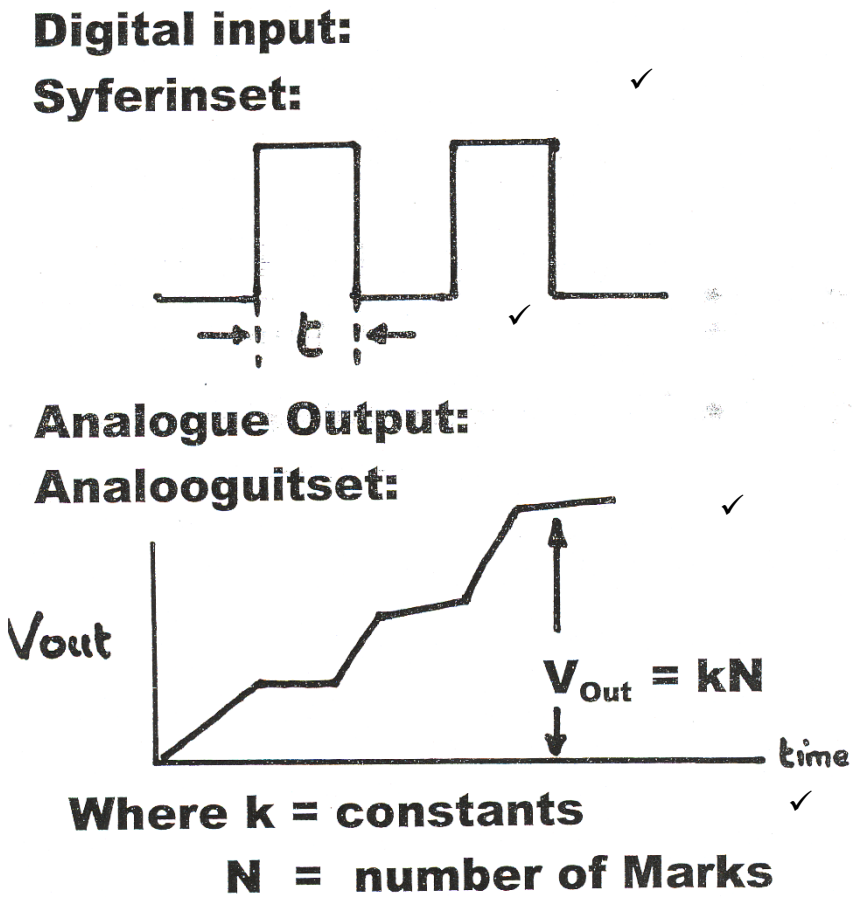
- Input voltage to be measured is applied to the integrator input.
- Capacitor C starts to charge up via input resistor R.
- During charging time, the pulse generator is off.
- When the voltage across capacitor C equals the reference voltage, the comparator provides an output to trigger the pulse generator.
- When triggered, the pulse generator provides a pulse to now discharge capacitor C.
- The charge and discharge rate of capacitor C provides the signal frequency for the frequency meter, which will be directly proportional to the input voltage being measured. (6)

2.3 Serial D/A converter



(4)

Waveforms of serial D/A converter



(4)

Operation of serial A/D converter:

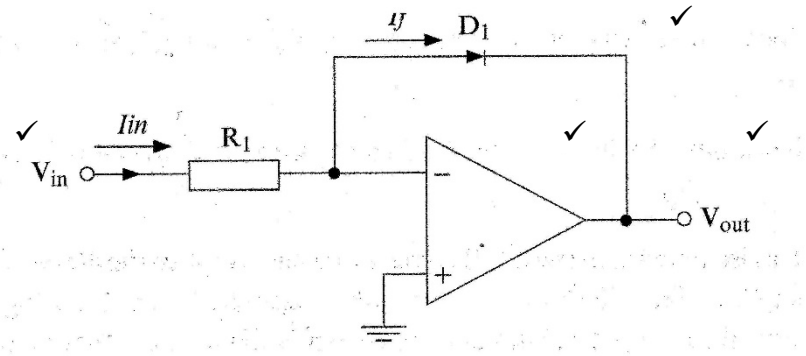
- When SW1 is closed, the integrator discharges capacitor C.
- Digital input voltage pulses are then applied to the input V_{in}.
- The voltage in the mark time of the pulse waveform charges the capacitor successively with each pulse applied during the time.
- The output voltage is proportional to N (the number of marks).
- SW1 is closed again to discharge capacitor C.
- The next string of input pulses is then applied and analogue output voltage is produced, which is proportional to the number of applied input pulses.

(Any 5 × 1) (5)

[25]

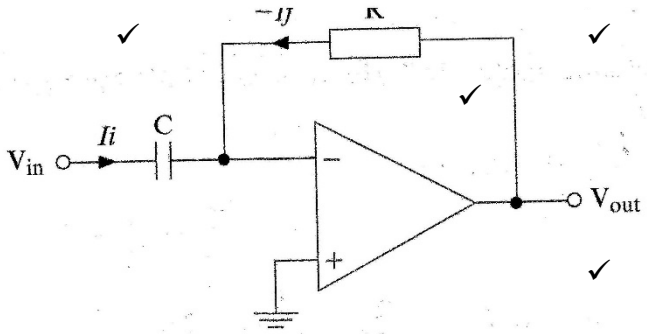
QUESTION 3

3.1 Logarithmic amplifier



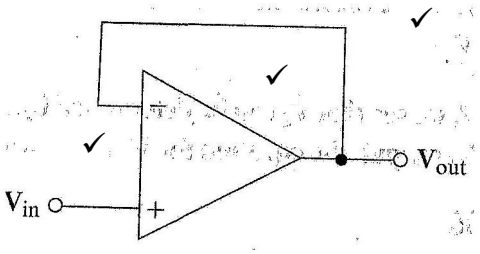
(4)

3.2 Differential amplifier



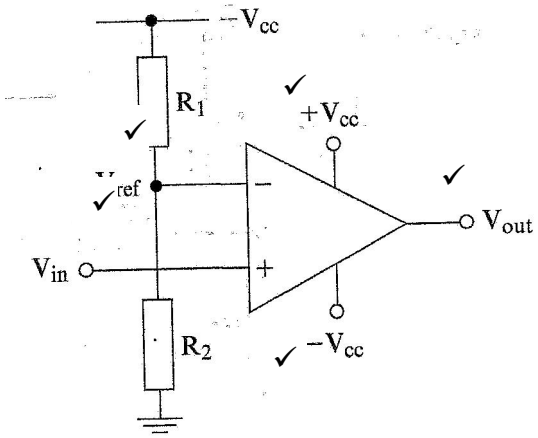
(4)

3.3 Impedance matching voltage follower



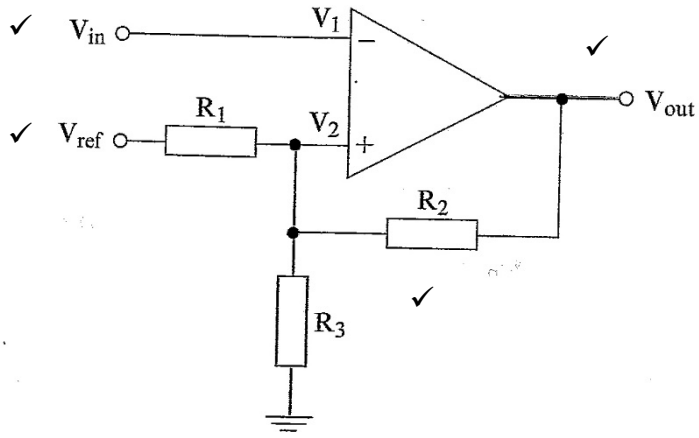
(3)

3.4 Voltage comparator



(5)

3.5 Schmitt trigger



(4)
[20]

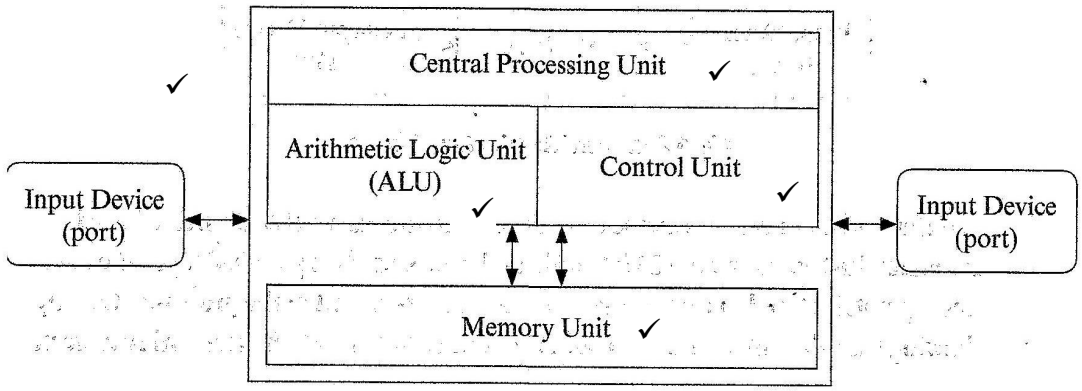
QUESTION 4

4.1 x = uyz + tuy
x = uy(t + z)✓

INSTRUCTION LOCATION	INSTRUCTION WORD		DESCRIPTION
	OP CODE	ADDRESS	
AACA	LOAD	F1C3	Load t✓
AACB	ADDA	F1C9	Add z✓
AACC	BRAN	AAD3✓	Branch if Acc. < 0✓
AACD	MULT	F1C4	Multiply by u✓
AACE	BRAN	AAD3	Branch if Acc. < O
AACF	MULT	F1C8✓	Multiply by y
AAD0	BRAN	AAD3	Branch if Acc. < O
AAD1	STOR	F1C7	Store in x✓
AAD2	OUTP		Output✓
AAD3	HALT		Halt✓

Note that other programming sequences are also accepted.
Either z or t can be loaded first.
Can be multiplied with either u or y first. (10)

4.2 Von Neumann architecture



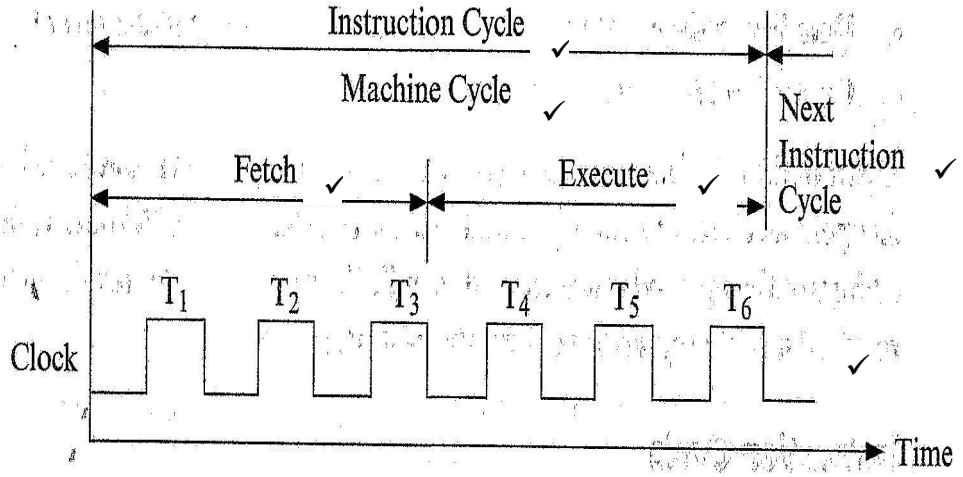
(5)

4.3
- The Harvard architecture uses separate storage (RAM and ROM)✓ for instructions and data,✓ making operations faster.✓
- The Von Neumann architecture uses only RAM✓ and the memory must be accessed twice during each machine cycle, making operations slower.✓ (5)

[20]

QUESTION 5

5.1



(6)

5.2
5.2.1 Data bus
5.2.2 Control bus
5.2.3 Control bus
5.2.4 Address bus
5.2.5 Input device
5.2.6 Output device
5.2.7 Input/Output port
5.2.8 Central processing unit (CPU)
5.2.9 Memory RAM and ROM

(9 × 1) (9)

[15]

TOTAL: 100

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