higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N5

(8080365)

24 November 2022 (X-paper)
09:00–12:00

Drawing instruments and nonprogrammable calculators may be used.

This question paper consists of 8 pages.

195Q1E2224

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
DIGITAL ELECTRONICS N5
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer all the questions.
2. Read all the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Start each section on a new page.
5. Calculation processes and calculated answers must be given in THREE fractional radix spaces, for example: 10, 101_2.
6. Use only a blue or black pen.
7. Write neatly and legibly.

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QUESTION 1

Various options are given as possible answers to the following questions. Choose the correct answer and write only the letter (A–D) next to the question number (1.1–1.10) in the ANSWER BOOK.

1.1 The Excess-3 BCD equivalent of the decimal number 729 is ...

A 0111 0010 1001.
B 0111 0101 1100.
C 1010 0101 1100.
D 1010 0010 1001.

1.2 When the output of a counter using SR flip-flops changes from 1 to 0, the input must be …

A S = X, R = 0.
B S = 0, R = 1.
C S = 0, R = X.
D S = 1, R = 0.

1.3 The simplification of the Boolean expression F_{ABC} = ABC + ABC + 1 is …

A ABC.
B ABC + ABC.
C ABC + 1.
D 1.

1.4 Which of the following is not part of the bipolar family?

A I^2L
B ECL
C NMOS
D TTL

1.5 *Fan out* is defined as …

A the maximum number of gate outputs that can be connected to a single gate input.
B the minimum number of gate outputs that can be connected to a single gate input.
C the maximum number of gate inputs that can be connected to a single gate output.
D the minimum number of gate inputs that can be connected to a single gate output.

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1.6 When an input to a TTL NAND gate is unused, the input can be …

A left unconnected.
B connected to a used input.
C tied to earth (0).
D tied to V_{CC} with a 1 kΩ resistor.

1.7 If the input to a tri-state inverter is 1 and the select input is 0, then …

A the output is in the high Z-state.
B the output is 1.
C the output is 0.

1.8 Which of the following TTL-series has the fastest switching speed?

A 74H00
B 74S00
C 74L00
D 74LS00

1.9 A typical output device is a/an …

A card reader.
B paper-tape reader.
C paper-tape punch.
D optical reader.

1.10 Outputs of open collector TTLs may be joined together using a ...

A totem-pole configuration.
B pull-up resistor.
C junction capacitor.
D Darlington pair.

(10 × 1) **[10]**

QUESTION 2

2.1 Convert each of the following numbers to their binary equivalents:
A = $6F,3_{16}$, B = $34,2_8$ and C = $16,75_{10}$ (3)

2.1.1 Find A × C. The multiplication must be performed in binary, and the answer must be converted to hexadecimal. (4)

2.1.2 Find B ÷ C. The division must be performed in binary, and the final answer must be converted to decimal. (5)

2.2 Find -34, 7_8 – 17, 5_8 using 2's complement and sign bits. The calculation must be performed in binary, and the final answer must be converted to hexadecimal. (7)
[19]

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QUESTION 3

3.1 Simplify the Karnaugh map below so that, in its reduced form, Boolean algebra cannot be performed on it to simplify it further.

F	$\overline{A}\overline{B}$	$\overline{A}B$	AB	$A\overline{B}$
$\overline{C}\overline{D}$	1	1	1	1
$\overline{C}D$	1	1		1
CD	1			1
$C\overline{D}$	1	1	1	1

(3)

3.2 Simplify the following function with the aid of a Karnaugh map:

$F = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + AB\overline{C}\overline{D} + AB\overline{C}D$ (8)

3.3 Use a truth table and Boolean algebra, or a Karnaugh map, and design the circuit of a parity-bit generator that can test a 3-bit word for even parity. Draw the circuit. (6)

[17]

QUESTION 4

4.1 With reference to TTL NAND gates, answer the following questions:

4.1.1 Draw the integrated circuit for a TWO-input TTL NAND gate with an open-collector output. (5)

4.1.2 What is the main DISADVANTAGE of open-collector devices as compared to totem-pole devices? (1)

4.1.3 Why should we use open-collector gates which require the addition of a pull-up resistor in order to function properly when we could use a gate with a totem-pole output instead? (1)

4.2 With reference to the 7 400 series IC: They operate reliably over the temperature range of 0 °C to 70 °C and have the following high- and low-state noise margins: V_{OH} = 2,4 V/min, V_{IH} = 2 V/min, V_{IL} = 0,8 V max and V_{OL} = 0,4 V max. Answer the following questions:

4.2.1 Define *noise immunity*.

4.2.2 Define *noise margin*.

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4.2.3 Calculate the high-state noise margin V_{NH}.

4.2.4 Calculate the low-state noise margin V_{NL}.

(4 × 2) (8)
[15]

QUESTION 5

Choose a description from COLUMN B that matches a term in COLUMN A. Write only the letter (A–E) next to the question number (5.1–5.5) in the ANSWER BOOK.

COLUMN A		COLUMN B	
5.1	Threshold	A	is the time it takes a D/A converter to settle within ± ½ LSB of its final value when a change occurs in the input
5.2	Accuracy		
5.3	Linearity	B	is a deviation from the ideal output of a D/A converter
5.4	Response time	C	are the minimum and maximum voltage levels which determine a logic state
5.5	Settling time	D	is a comparison between the actual output and the expected output
		E	is the reciprocal of the number of discrete steps in the output signal or the number of bits that are converted

(5 × 1) **[5]**

QUESTION 6

With reference to memories, answer the following questions:

6.1 Define *access time*. (2)

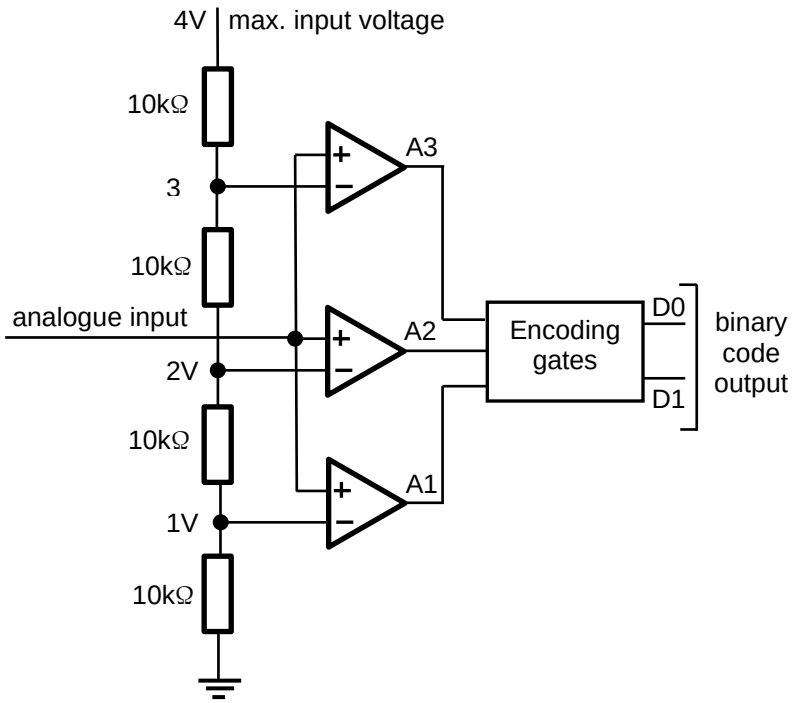
6.2 Draw a block diagram of a static bipolar memory cell. (7)

6.3 Explain the operation of the static bipolar memory cell in QUESTION 6.2. (4)
[13]

QUESTION 7

With reference to digital-to-analogue and analogue-to-digital converters, answer the following questions.

7.1 Identify the converter shown below:



(1)

7.2 Explain the operation of the converter shown in QUESTION 7.1 by redrawing and completing the following table in your ANSWER BOOK:

Analogue input voltage			Comparator outputs			Binary outputs	
			A1	A2	A3	D1	D0

(4)

7.3 State the major DISADVANTAGE of the converter shown in QUESTION 7.1. (1)

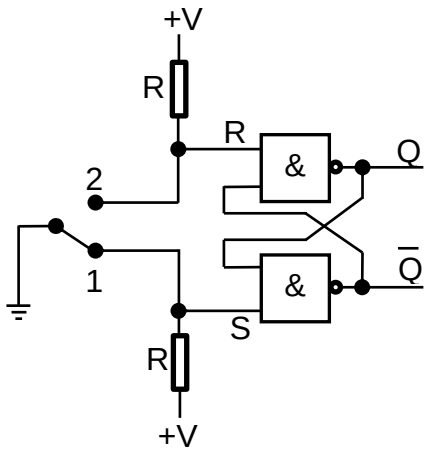
7.4 State the major ADVANTAGE of the converter shown in QUESTION 7.1. (1)

[7]

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QUESTION 8

The FIGURE below shows a circuit for *contact bounce elimination* using an SR latch.



Briefly explain the operation of the above circuit with

8.1 the switch in position 1. (1)

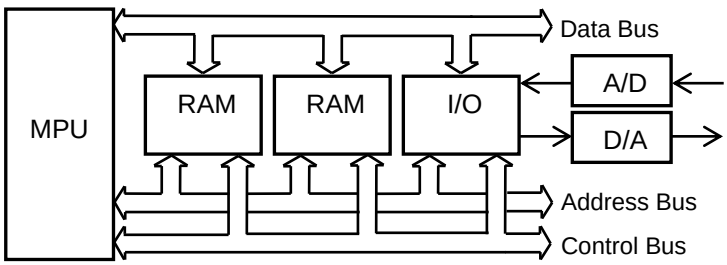
8.2 the switch in position 2. (1)

8.3 the connection in position 2 broken due to contact bounce. (2)
[4]

QUESTION 9

With reference to input and output devices, answer the following questions.

9.1 Name the following block diagram:



(1)

9.2 Describe the function of the *data bus*. (3)

9.3 Describe the function of the *address bus*. (3)

9.4 Describe the function of the *control bus*. (3)
[10]

TOTAL: 100

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