higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N5

24 November 2022

This marking guideline consists of 7 pages.

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QUESTION 1

1.1	C
1.2	B
1.3	D
1.4	C
1.5	C
1.6	C
1.7	A
1.8	B
1.9	C
1.10	B

(10 × 1) **[10]**

QUESTION 2

2.1 $6F,3_{16}$ = 0 1 1 0 1 1 1 1, 0 0 1 1_2 ✓
$34,2_8$ = 1 1 1 0 0, 0 1_2 ✓
$16,75_{10}$ = 1 0 0 0 0, 1 1_2 ✓ (3)

2.1.1

```
                    1 1 0 1 1 1 1 0 0 1 1
                              1 0 0 0 0 1 1   ×
                    1 1 0 1 1 1 1 0 0 1 1
                1 1 0 1 1 1 1 0 0 1 1         ✓✓
1 1 0 1 1 1 1 0 0 1 1                         +
1 1 1 0 1 0 0 0 1 1 0, 0 1 1 0 0 1            ✓
```

Answer: 1 1 1 0 1 0 0 0 1 1 0, 0 1 1 0 0 1_2 = $746,64_{16}$✓ (4)

2.1.2

```
                                  1, 1 0 1        ✓✓
1 0 0 0 0 1 1 | 1 1 1 0 0 0 1, 0 0 0
                1 0 0 0 0 1 1 -
                  1 0 1 1 1 0 0                   ✓
                  1 0 0 0 0 1 1 -
                      1 1 0 0 1 0 0
                      1 0 0 0 0 1 1 -
                        1 0 0 0 0 1               ✓
```

Answer: 1, 1 0 1_2 = 1, 625_{10}✓ (5)

2.2 $34, 7_8$ = 1 1 1 0 0, 1 1 1_2 ✓
$17, 5_8$ = 1 1 1 1, 1 0 1_2 ✓

```
                1 0 1 1 1 0 0, 1 1 1
                1 0 0 1 1 1 1, 1 0 1 -
2/C             1 1 1 0 0 0 0, 0 1 1     ✓
2/C             1 1 0 0 0 1 1, 0 0 1 +   ✓
Ignore Carry  1 1 0 1 0 0 1 1, 1 0 0     ✓
2/C             - 1 0 1 1 0 0, 1 0 0     ✓
```

Answer: - 1 0 1 1 0 0, 1 0 0_2 = - 2C, 8_{16} ✓ (7)

[19]

QUESTION 3

3.1 F = $\overline{B}$✓ + $\overline{D}$✓ + $\overline{A}.\overline{C}$✓

Both the OR signs must be included for the answer to be marked. (3)

3.2

	$\overline{A}\,\overline{B}$	$\overline{A}\,B$	$A\,B$	$A\,\overline{B}$
$\overline{C}\,\overline{D}$		1	1	1
$\overline{C}\,D$	1	1	1	1
$C\,D$				
$C\,\overline{D}$	1			

✓✓ for posting correctly

✓✓ for grouping correctly

F = $\overline{A}\,\overline{B}C\,\overline{D} + \overline{C}\,D + B\,\overline{C} + A\,\overline{C}$ ✓✓✓✓

OR

	$\overline{C}\,\overline{D}$	$\overline{C}\,D$	$C\,D$	$C\,\overline{D}$
$\overline{A}\,\overline{B}$		1		1
$\overline{A}\,B$	1	1		
$A\,B$	1	1		
$A\,\overline{B}$	1	1		

✓✓ for posting correctly

✓✓ for grouping correctly

F = $\overline{A}\,\overline{B}C\,\overline{D} + \overline{C}\,D + B\,\overline{C} + A\,\overline{C}$ ✓✓✓✓

All three the OR signs must be included for the answer to be marked. (8)

3.3 F (A,B,C) = ∑ m (1;2;4;7)

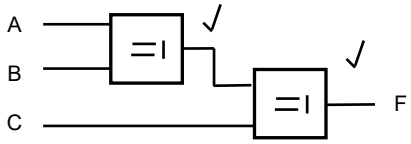
$F = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + A\,B\,C$✓
$F = \bar{A}\,(\bar{B}\,C + B\,\bar{C}) + A(\bar{B}\,\bar{C} + B\,C)$✓
$F = \bar{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$ ✓
$F = A \oplus B \oplus C$✓

OR

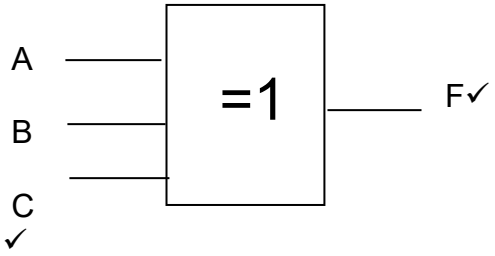
F	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$		**1**		**1**
C	**1**		**1**	

✓✓ for posting correctly

$F = A \oplus B \oplus C$✓✓



OR

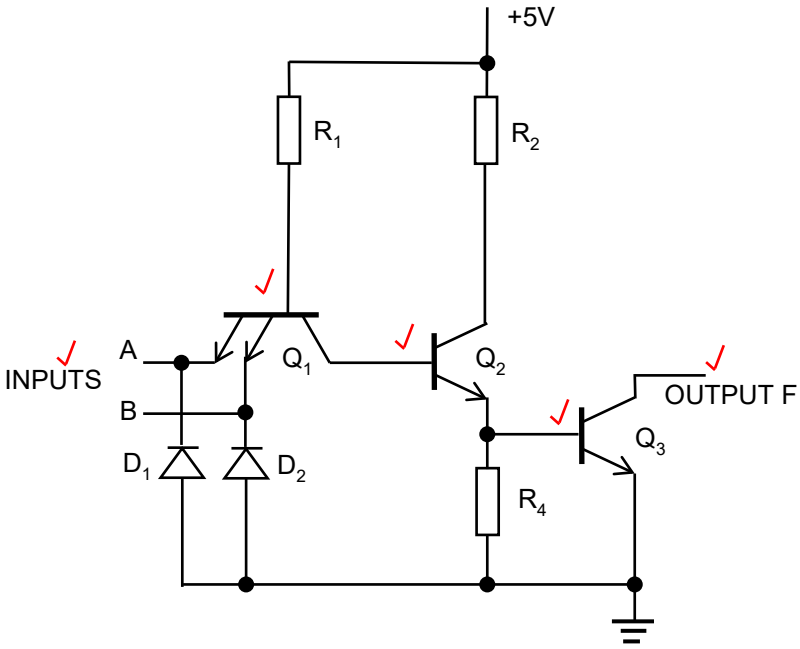


✓

(6)
[17]

QUESTION 4

4.1 4.1.1



(5)

4.1.2 Slow switching speed (1)

4.1.3
- Open-collector outputs can be tied directly together which results in the logical ANDING of the outputs.
- The equivalent of an AND gate can be formed by simply connecting the outputs. (Any 1 × 1) (1)

4.2 4.2.1 Noise immunity – is the maximum noise voltage a TTL device can withstand✓ without a false change in the output.✓

4.2.2 Noise margin – is the difference between✓ the tolerable output and input ranges of the gate.✓

OR

It is the voltage swing✓ between the two binary conditions.✓

4.2.3 $V_{NH} = V_{OH\ MIN} – V_{IH\ MIN}$
$= 2,4\ V – 2,0\ V$ ✓
$= 0,4\ V$ ✓

4.2.4 $V_{NL} = V_{IL\ MAX} – V_{OL\ MAX}$
$= 0,8\ V – 0,4\ V$ ✓
$= 0,4\ V$ ✓

(4 × 2) (8)
[15]

QUESTION 5

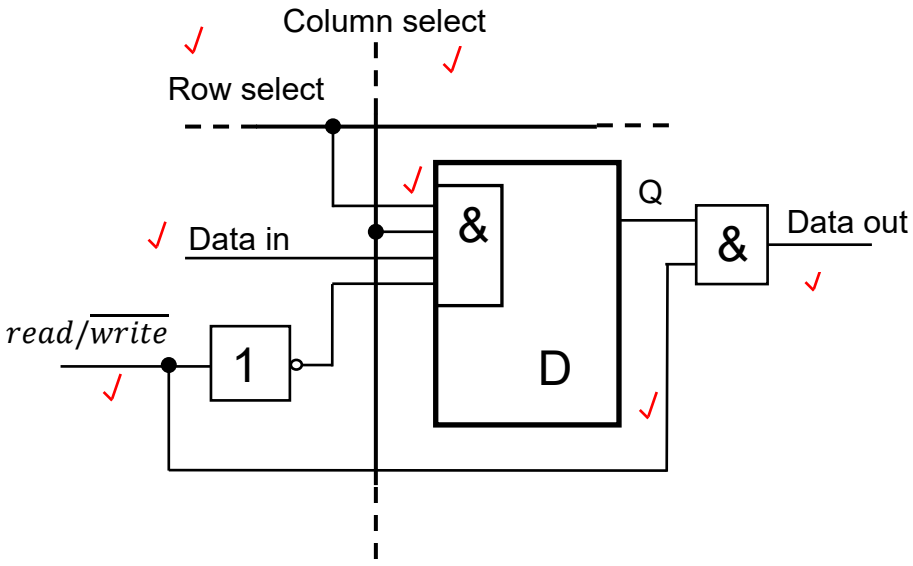
5.1 C
5.2 D
5.3 B
5.4 E
5.5 A

(5 × 1) **[5]**

QUESTION 6

6.1 The interval of time required to locate and store/retrieve data from a specified location. (2)

6.2



(7)

6.3 A cell is selected by a '1' on row and column select lines.✓ When the read/write is '0' (write), the input data is written into the cell by setting the latch for a '1' or resetting the latch for a '0'.✓ When the read/write line is '1' (read), the latch is unaffected,✓ but the stored data bit Q is gated to the data output line.✓

(4)
[13]

QUESTION 7

7.1
- Parallel comparator A/D converter **or**
- Simultaneous A/D converter **or**
- Flash A/D converter

(Any 1 × 1) (1)

7.2

Analogue input voltage			Comparator outputs			Binary outputs		
			A1	A2	A3	D1	D0	
0	to	1	0	0	0	0	0	✓
1	to	2	1	0	0	0	1	✓
2	to	3	1	1	0	1	0	✓
3	to	4	1	1	1	1	1	✓

(4)

7.3 The use of an excessive number of comparators for a high resolution.✓

OR

The use of an excessive number of op-amps for a high resolution.✓ (1)

7.4 It is simple in concept and fast. (1)

[7]

QUESTION 8

S is low and the Q-output is low.✓ When switch position moves to position 2, S is high, R is low, and the Q-output is high.✓ If the connection with position 2 has been broken due to contact bounce, S is high and R is high✓ while Q is keeping S high, and $\overline{Q}$ is keeping R low. In this condition, the output voltage Q will not be changed.✓ **[4]**

QUESTION 9

9.1 The components of a microcomputer. (1)

9.2 The data bus is a bi-directional bus,✓ used for transporting data from the MPU✓ to the memory and I/O devices, and back to the MPU.✓ (3)

9.3 The address bus is a uni-directional bus,✓ used for transporting address codes from the MPU✓ to the memory and I/O devices.✓ (3)

9.4 The control bus is a bi-directional bus,✓ used for transporting control codes from the MPU✓ to the memory and I/O devices, and back to the MPU.✓ (3)

[10]

TOTAL: 100

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