higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

DIGITAL ELECTRONICS N4

29 November 2022

This marking guideline consists of 7 pages.

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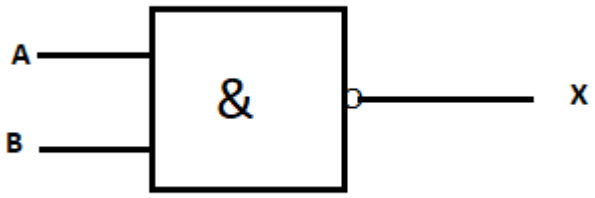
QUESTION 1

1.1 Binary coded decimal (1)

1.2 X-3 BCD (1)

1.3



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

$Q = \overline{AB}$ (3)

1.4 1.4.1 X
1.4.2 $\overline{X} + Y$
1.4.3 X
1.4.4 $\overline{X}$
1.4.5 1

(5 × 1) (5)

1.5 In synchronous switching, flip-flops are clocked simultaneously, while in asynchronous switching, the output of one flip-flop serves as the clock of the next flip-flop. (2)

1.6 0111110_{gray} (1)

1.7 Two selected lines (1)

1.8 A full adder has a carry input and a half adder has no carry input. (2)
[16]

QUESTION 2

2.1 $7,5_8 = 111,101_2$ $0111,101_2$✓
$9,125_{10} = 1001,001_2$ 2's/complement $\underline{0110,111_2}$✓
$1110,100_2$✓
No carry get 2's complement $-0001,100_2$ ✓✓
Answer = $-1,4_8$✓ (6)

2.2 $12,125_{10} = 1110,001_2$✓
$6,4_8 = 110,100_2$ ✓
10,001✓
110100 $\sqrt{1110001,000}$
1101000
0001001000
0000110100
0000010100✓✓
Answer = $10,001_2$
$= 2,125_{10}$✓ (6)

2.3 $11,375_{10} = 1011,011_2$✓
$5,2_8 = 101,01_2$✓

1011,011
× 101,01
1011011
101101100
10110110000
$111011,10111_2$ ✓✓✓
Answer = $73,56_8$✓ (6)

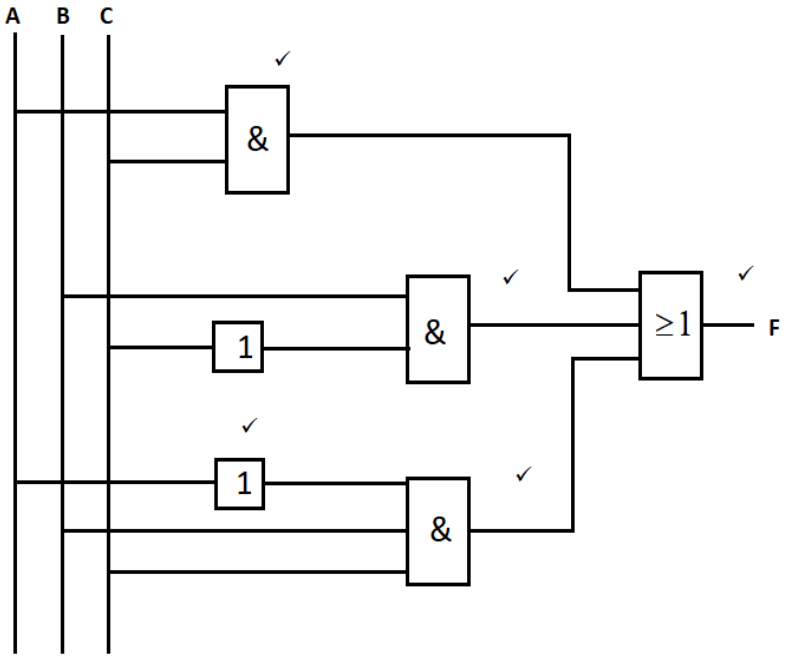
2.4 $-17,25_{10} = 010001,01_2$ 1's complement 101110,10✓
$14,75_{10} = 001110,11_2$ 1's complement 110001,00✓

101110,10
110001,00
011111,10
+1
011111,11✓✓
-100000,00✓

Answer = -40_8✓ (6)
[24]

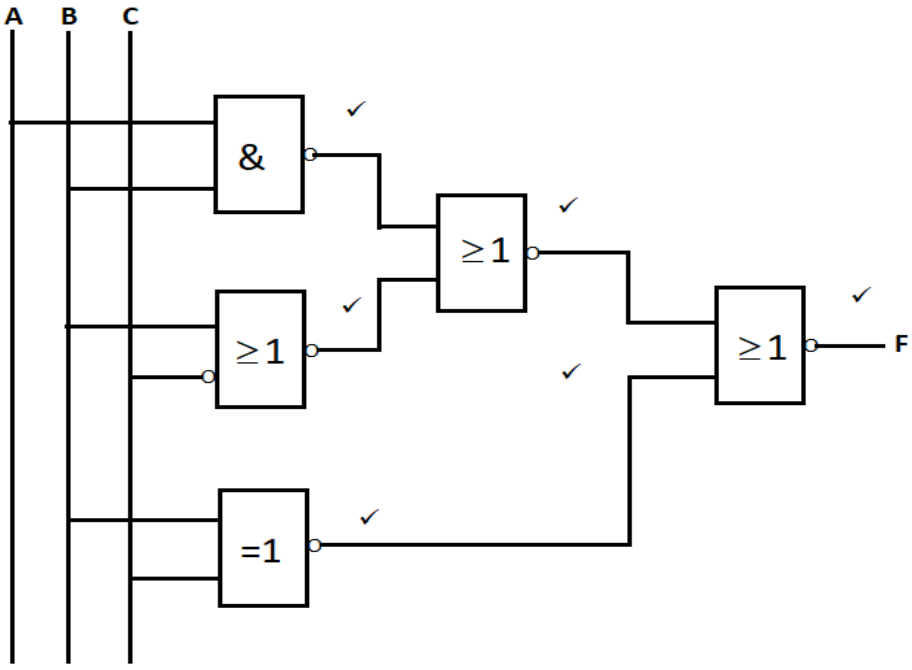
QUESTION 3

3.1 3.1.1



(5)

3.1.2



(6)

3.2 3.2.1

$$F = A\,B\,C + \overline{A}\,\overline{B}\,C + A\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C}$$

$$F = \overline{A}\,(\overline{B}C + B\overline{C}) + A\,(\overline{B\overline{C}} + BC) \checkmark$$

$$= A\,(\overline{(B \oplus C)} + A\,(\overline{B \oplus C}) \checkmark$$

$$LET\ B \oplus C = K \checkmark$$

$$\therefore\ F = \overline{A}K + A\overline{K} \checkmark$$

$$= A \oplus K \checkmark$$

$$= A \oplus B \oplus C \checkmark$$

(6)

3.2.2 $F = \overline{X + \overline{X}Y + \overline{Y + Z}}$

$= \overline{(X + \overline{X}Y)}.(Y + Z)$ ✓

$= \overline{(X + Y)}.(Y + Z)$ ✓

$= \overline{X}.\overline{Y}.(Y + Z)$ ✓

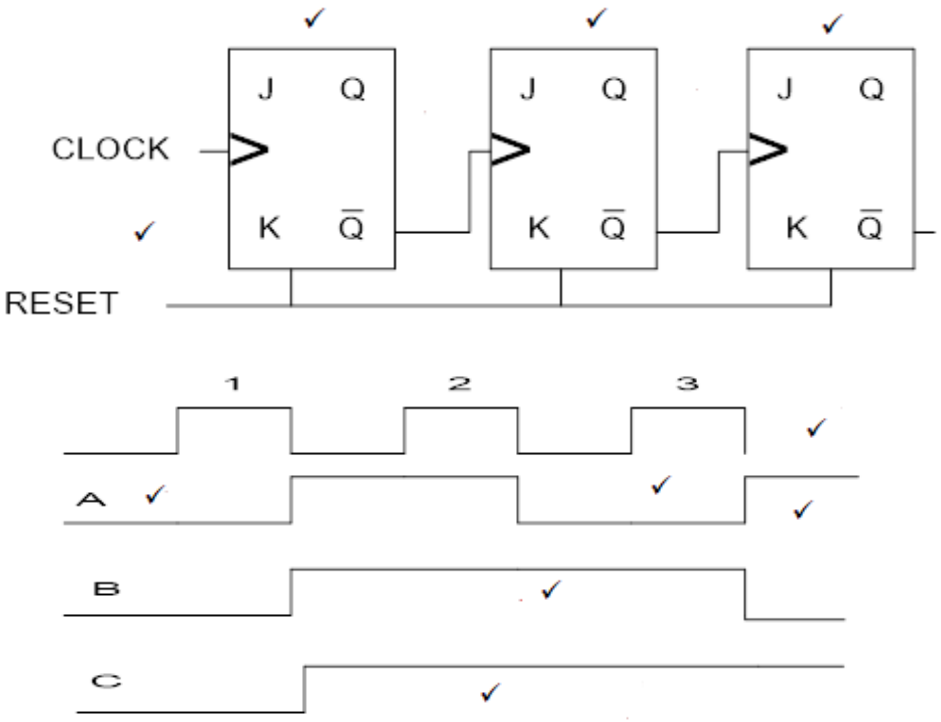
$= 0 + \overline{X}.\overline{Y}..Z$ ✓

$= \overline{X}.\overline{Y}.Z$ ✓

(5)
[22]

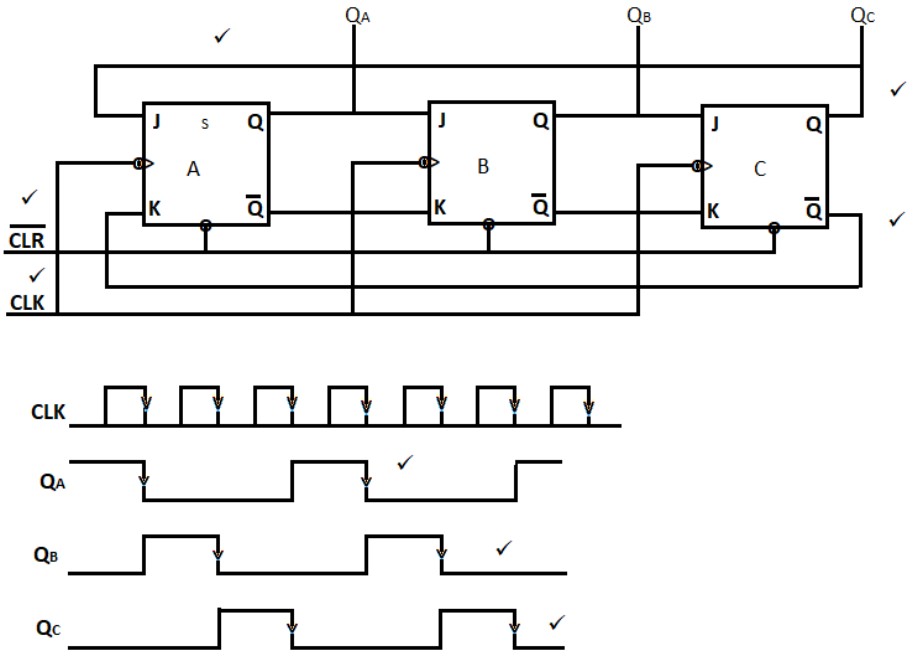
QUESTION 4

4.1



(10)

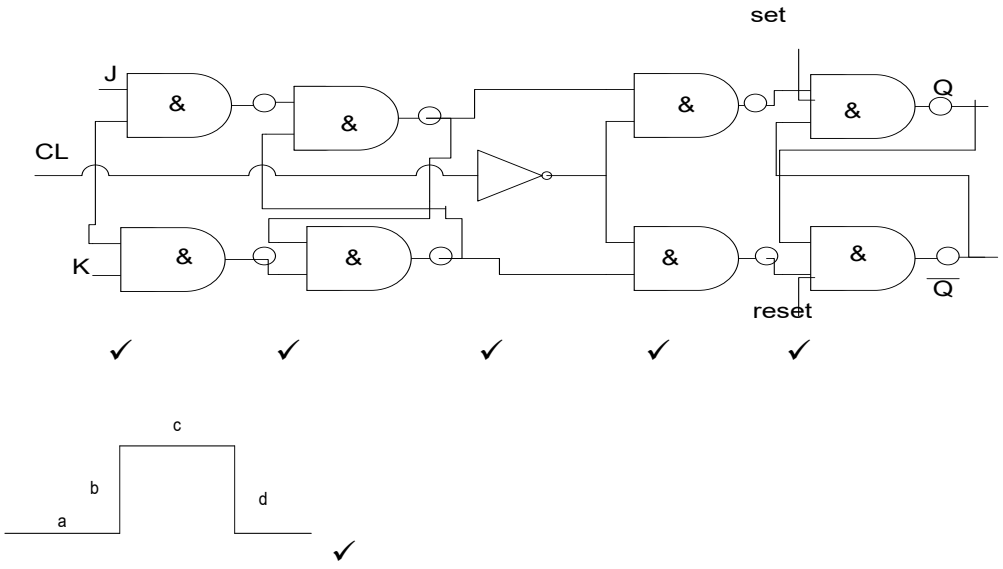
4.2



(8)
[18]

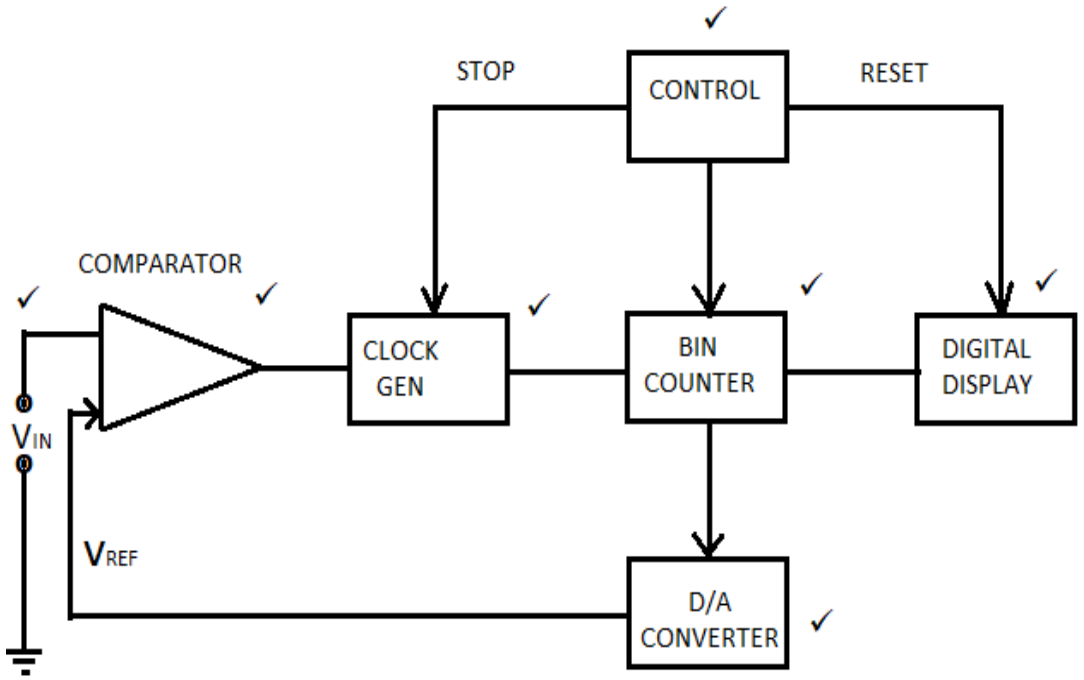
QUESTION 5

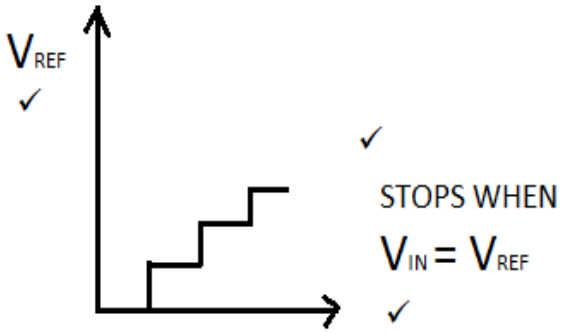
5.1



- At (a) the pulse is at logic 0, the master is off and the slave is on.
- At (b) the OR gate triggers before the master changes state because of the current-sinking resistor.
- At (c) the pulse is at logic 1, the master is on and the slave is off.
- At (d) the OR gate triggers, passing the state of the master to the slave because of the current-sinking resistor, and therefore the slave is receptive to the master on the trailing edge. (10)

5.2





(10)
[20]

TOTAL: 100

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