higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

21 November 2022 (X-paper)
09:00–12:00

Calculators may NOT be used. Drawing instruments may be used.

This question paper consists of 5 pages.

112Q1E2221

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer all the questions.
2. Read all the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. All the sketches and diagrams must be large, clear and neat.
5. Keep questions and subsections of questions together.
6. All calculations must be shown.
7. Start each question on a new page.
8. Questions must be answered in a blue or black pen, and all drawings must be done in pencil.
9. Write neatly and legibly.

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QUESTION 1

1.1 Name the THREE gates that will produce an output of logic 1 when one of the two inputs is on logic 1. (3)

1.2 Define the operation of the following gates:

1.2.1 A two-input exclusive OR-gate (2)

☆ 1.2.2 A NOT-gate (2)

1.3 1.3.1 Draw the truth table of the logic gates mentioned in 1.2.1 and 1.2.2 above. (4)

1.3.2 Draw the IEC – circuit symbols of the gates mentioned in 1.2.1 and 1.2.2 above. (2)

1.4 Convert the following decimal numbers to binary number systems

1.4.1 36 (2)

1.4.2 15 (2)

1.5 Perform the following arithmetic calculation in binary. Give the final answers in decimal system.

1.5.1 36 + 15 (3)

1.5.2 36 - 15 (3)

1.6 Give the IEC symbols of the following circuits:

1.6.1 The full adder ☆

1.6.2 The full subtractor

(2 × 1) (2)

[25]

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QUESTION 2

2.1 The table below consists of 4-bit weighted codes. Complete the table by writing only the correct answer next to the question number (2.1.1–2.1.9) in the ANSWER BOOK.

☆

Decimal	2421	4221
0	0000	0000
1	0001	**2.1.1**
2	**2.1.2**	0010
3	0011	**2.1.3**
4	**2.1.4**	1000
5	1011	**2.1.5**
6	**2.1.6**	1100
7	1101	**2.1.7**
8	**2.1.8**	1110
9	1111	**2.1.9**

TABLE 1 (9 x1) (9)

2.2 What are codes used for? (1)

2.3 Give THREE examples of weighted codes. (3)

2.4 When is a code said to be a self-complementing code? (2)

2.5 Draw a truth table indicating the conversion of a BCD to Excessive 3 code. (10)
[25]

QUESTION 3

3.1 What is the difference between *primary* and *secondary* storage/memory? (4)

3.2 Give THREE examples of secondary memory/storage. (3)

3.3 What does the acronym CD stand for? (1)

3.4 Study FIGURE 1 below, and draw the appropriate logic circuit that is associated with it.

☆

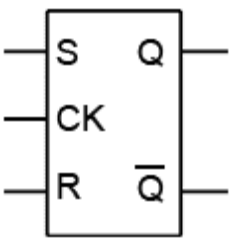


FIGURE 1 (5)

3.5 Complete the following table in relation to logic gates. Write only the correct answer next to the question number (3.5.1–3.5.6) in the ANSWER BOOK.

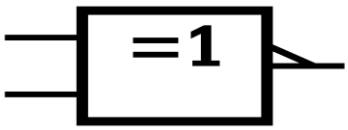
<table>
<tr><th>LOGIC GATE</th><th>IEC SYMBOL</th><th>TRUTH TABLE</th></tr>
<tr><td>NAND</td><td>3.5.1 (2)</td><td>3.5.2 (2)</td></tr>
<tr><td>3.5.3 (2)</td><td>
</td><td>3.5.4 (2)</td></tr>
<tr><td>3.5.5 (2)</td><td>3.5.6 (2)</td><td>
<table>
<tr><th>A</th><th>B</th><th>Z</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
</table>

TABLE 2

(12)
[25]

☆

QUESTION 4

4.1 How many flip-flops are required to construct a shift register that is capable of storing a six-bit binary number? (1)

4.2 A decade counter is connected in series with a two-bit counter.

Given the above circuit, how many clock pulses can be counted? (2)

4.3 Draw a neat, labelled diagram of a parallel-in/series-out shift register. (10)

4.4 Indicate whether the following statements are TRUE or FALSE. Choose the answer and write only 'true' or 'false' next to the question number (4.4.1–4.4.5) in the ANSWER BOOK.

4.4.1 If only a “counter” is mentioned, it implies a down counter

4.4.2 In asynchronous counter, the output of one flip-flop is used to clock the input of the following flip-flop. ☆

4.4.3 D Flip-flop is the modified form of clocked R S flip-flop.

4.4.4 The series in-series out shift register is actually the delay register.

4.4.5 A register is defined as the group of flip-flops suitable for storing decimal information.

(5 × 1) (5)

4.5 Name THREE basic control pulses used by flip-flops (3)

4.6 Differentiate between a Jonson counter and the Ring counter. (4)

[25]

TOTAL: 100