higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

(8080262)

27 November 2023 (X-paper)
09:00–12:00

Calculators may NOT be used.
Drawing instruments may be used.

This question paper consists of 6 pages.

110Q1E2327

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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA

NATIONAL CERTIFICATE
LOGIC SYSTEMS N2
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer all the questions.
2. Read all the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. Start each question on a new page.
5. All the sketches and diagrams must be large, clear and neat.
6. Keep questions and subsections of questions together.
7. Questions must be answered in a blue or black pen and all drawings with a pencil.
8. All calculations must be shown.
9. Write neatly and legibly.

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QUESTION 1

1.1 Various options are given as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question number (1.1.1–1.1.5) in the ANSWER BOOK.

1.1.1 In the binary system, the sum of 1011_2 and 1101_2 is …

A 10111_2
B 1111_2
C 11000_2
D 10001_2

1.1.2 When the binary number 11_2 is subtracted from 10000_2, the answer is …

A 1111_2
B 1000_2
C 1110_2
D 1101_2

1.1.3 If a binary number is 100_2 , then the MSD is …

A 0
B 1
C 1 and 0
D 1 or 0

1.1.4 When the decimal number 87 is converted to binary, it becomes

A 111101_2
B 010010_2
C 1010111_2
D 1110101_2

1.1.5 With four binary bits, what is the largest decimal equivalent?

A 15
B 8
C 4
D 2

(5 × 1) (5)

1.2 Perform the following arithmetic calculations below in the binary system, then convert each answer to decimal. Show all conversions and calculations clearly.

1.2.1 $13_{10} + 11_{10}$

1.2.2 $1101_2 \times 110_2$

1.2.3 $27_{10} - 14_{10}$

(3 × 5) (15)

1.3 In order to add two or more bits, a circuit called full adder must be developed. This circuit will be able to cater for the C_{in} which is from the previous operation.

Draw a circuit of a FULL ADDER consisting of two half adders, using OR gate, AND gates, and exclusive OR gates. (5)

[25]

QUESTION 2

2.1 Describe the following codes:

2.1.1 Non-weighted code (2)

2.1.2 Weighted code (1)

2.1.3 Self-complementing code (3)

2.2 Use the decimal number 854_{10} and convert it to the following codes:

2.2.1 8421 BCD code (4)

2.2.2 2421 BCD code (4)

2.2.3 XS3 code (5)

2.3 A central processor used to monitor the data converts decimal number into 2421 binary code.

Draw a circuit that will carry out this conversion. (6)

[25]

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QUESTION 3

3.1 Provide a statement that best describes ROM. (2)

3.2 What does the acronym EPROM stand for? (1)

3.3. Choose a term from COLUMN B that matches a description in COLUMN A. Write only the letter (A–L) next to the question number (3.4.1–3.4.4) in the ANSWER BOOK.

COLUMN A		COLUMN B	
3.3.1	It stores data on a permanent bases.	A	ROM
3.3.2	For this type of memory, data cannot be written on it.	B	RAM
		C	DVD RW
3.3.3	It is an example of the volatile memory that operates at high speeds.	D	Secondary memory
3.3.4	It's a disc in which data can be written and erased again and again.	E	Primary memory

(1 × 4) (4)

3.4 Define the following terms in relation to digital systems:

3.4.1 AND gate

3.4.2 OR gate

(2 × 2) (4)

3.5 With reference to a positive logic clock pulse, what is meant by *leading edge* and *trailing edge*? (3)

3.6 Name ANY TWO applications of flip-flop. (2)

3.7 Describe how does a RS flip-flop with a NAND latch operates. (5)

3.8 Draw a truth table for the clocked RS flip-flop with a NAND latch. (4)

[25]

QUESTION 4

4.1	Explain the term *shift register*.	(2)
4.2	Give the TWO basic functions of a register.	(2)
4.3	Give another name for asynchronous counter.	(1)
4.4	List FOUR aspects that are used to differentiate between the types of counters.	(4)
4.5	Shift registers are mainly classified into four types.	
4.5.1	Name the FOUR types of shift registers	(4)
4.5.2	State ONE application of TWO types of shift register mentioned in 4.5.1	(2)
4.6	Draw a neatly labelled diagram of a 4-bit asynchronous binary counter consisting of JK flip-flops.	(10)
		[25]

TOTAL: 100

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