higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

27 November 2023

This marking guideline consists of 6 pages.

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QUESTION 1

1.1 1.1.1 C
1.1.2 D
1.1.3 B
1.1.4 C
1.1.5 A

(5 × 1) (5)

1.2 1.2.1 $13_{10} + 11_{10}$

	2^3	2^2	2^1	2^0
	8	4	2	1
13	1	1	0	1

✓

	2^3	2^2	2^1	2^0
	8	4	2	1
11	1	0	1	1

✓

	1	1	0	1
+	1	0	1	1
1	1	0	0	0

✓

$1\ 1\ 0\ 0\ 0_2 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0$ ✓
$= 16 + 8 + 0 + 0 + 0$
$= 24_{10}$ ✓

1.2.2 $1101_2 \times 110_2$

			1	1	0	1	
		x		1	1	0	✓
			0	0	0	0	
		1	1	0	1		
+	1	1	0	1			✓
1	0	0	1	1	1	0	✓

$1001110_2 = 1 \times 2^6 + 0 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$ ✓
$= 64 + 0 + 0 + 8 + 4 + 2 + 0$
$= 78_{10}$ ✓

1.2.3 $27_{10} - 14_{10}$

	2^4	2^3	2^2	2^1	2^0
	16	8	4	2	1
27	1	1	0	1	1

✓

	2^3	2^2	2^1	2^0
	8	4	2	1
14	1	1	1	0

✓

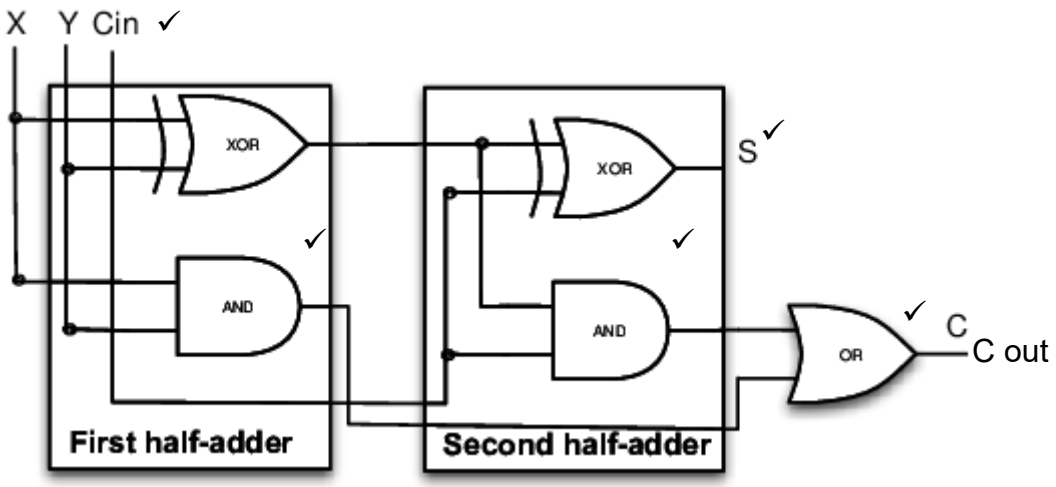
	1	1	0	1	1
–		1	1	1	0
		1	1	0	1

✓

$1\ 1\ 0\ 1_2 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^\circ$ ✓
$= 8 + 4 + 0 + 1$
$= 13_{10}$ ✓

(3 × 5) (15)

1.3



(5)
[25]

QUESTION 2

2.1 2.1.1 Non-weighted code is a code whereby the value of the position of every binary digit✓ cannot be specified, or does not have weight value.✓ (2)

2.1.2 Weighted code is a code whereby the value of the position of every binary digit can be specified.✓ (1)

2.1.3 Self-complementing code is a code whereby the coded number is to be subtracted from 9✓ and the result is the compliment of that number✓. This means that all zeros in the number would change to one and all the ones would change to a zero.✓ (3)

2.2 2.2.1

8	5	4
8421	8421	8421
1000 ✓	0101 ✓	0100 ✓

$854 = 100001010100_{8421BCD}$ ✓ (4)

2.2.2

8	5	4
2421	2421	2421
1110 ✓	1011 ✓	0100 ✓

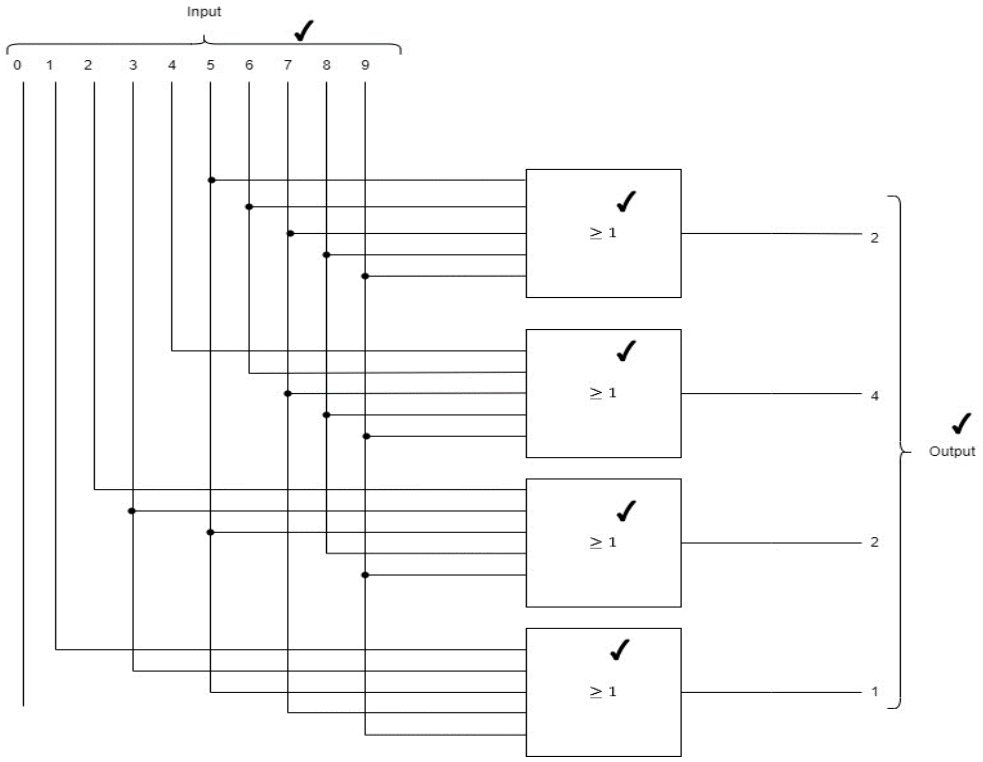
$111010110100_{2421BCD} = 854_{10}$ ✓ (4)

2.2.3 (5)

8	5	4
+3	+3	+3
11	8	7 ✓
8421	8421	8421
1011 ✓	1000 ✓	0111 ✓

$854_{10} = 101110000111_{XS3CODE}$ ✓

2.3



[25]

QUESTION 3

3.1 Read-Only Memory is a non-volatile memory.✓ This memory retains information even if the power supply is removed.✓ (2)

3.2 Erasable Programmable Read-Only Memory✓ (1)

3.3
3.3.1 D
3.3.2 A
3.3.3 B
3.3.4 C

(4 × 1) (4)

3.4 3.4.1 The output of an AND gate will be a logic 1 only if both of the inputs are at logic 1✓, otherwise the output will be logic 0. ✓

3.4.2 The output of an OR gate will be a logic 1 only if one or both of the inputs are at logic 1✓, otherwise the output will be logic 0.✓

(2 × 2) (4)

3.5 For positive logic clock pulse we define the low to high transition✓ as the *leading edge* of the clock signal✓, while the transition from high to low is called the *clock trailing edge*.✓ (3)

3.6
- In frequency division and counting circuits
- For data storage and transfer circuits
- For switching debouncing
- For synchronising asynchronous inputs
- For identification of edges of synchronous inputs (Any 2 × 1) (2)

3.7
- The two NAND gates at the inputs couple the R and S inputs to the flip-flop inputs.
- The NAND gates are controlled by means of the clock wave.
- When the clock is 0, the two NAND gates produce a 1 at their outputs regardless of the R and S status.
- As soon as the clock changes to 1 the two gates are opened
- and what follows depends on the values of R and S which are fed to the RS flip-flop. (5)

3.8

Inputs		Outputs		Action
S	R	Q	Q'	
0	0	Q_n	Q'_n ✓	No change
0	1	0	1 ✓	Reset
1	0	1	0 ✓	Set
1	1	0	0 ✓	Undefined

(4)

[25]

QUESTION 4

4.1 A shift register is a group of flip-flops arranged in such a way that binary numbers stored in the flip-flops✓ are shifted from one flip-flop to the next for every clock pulse. ✓ (2)

4.2
- Data storage
- Data movement (2)

4.3 Serial or ripple counter (1)

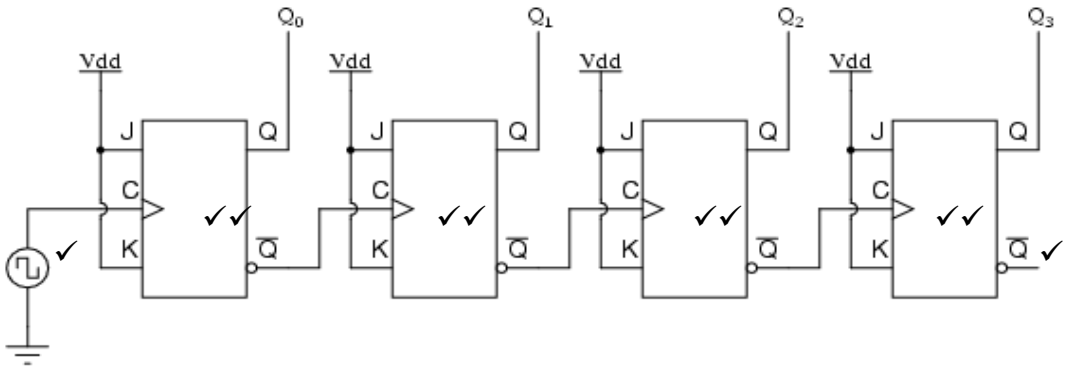
4.4
- Clock (i.e., synchronous or asynchronous)
- Counts (i.e., binary or decade)
- Clock trigger (i.e., positive or negative edge)
- Count direction (i.e., up, down or up/down) (4)

4.5 4.5.1
- Serial-In Serial-Out
- Serial-In Parallel Out
- Parallel-In Serial-Out
- Parallel-In Parallel-Out (4)

4.5.2
- Serial-In Serial-Out – operates as delay element
- Serial-In Parallel-Out – used in communication lines to change serial data to parallel information
- Parallel-In Serial-Out – used in communication relines converts parallel data to serial data
- Parallel-In Parallel-Out – used as temporary storage

(Any 2 × 1) (2)

4.6



(10)
[25]

TOTAL: 100

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